NCR Kit Information

3279-K010 80386 Upgrade

FEDERAL COMMUNICATIONS COMMISSION (FCC) RADIO FREQUENCY INTERFERENCE STATEMENT

WARNING

This equipment has been certified to comply with the limits for a Class B computing device, persuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc,) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

Information to User

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, it may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate the computer with respect to the receiver
- Move the computer away from the receiver
- Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

The NCR Corporation (NCR) is not responsible for any radio or television interference caused by unauthorized modifications of this equipment or the substitution or attachment of connecting cables and equipment other than those specified by NCR. The correction of interferences caused by such unauthorized modification, substitution or attachment will be the responsibility of the user.

Only shielded data cables may be used with this system.

80386 Upgrade

This kit is designed to upgrade your PC with an 80386 processor and the required memory to operate the processor. A memory of 1 MB is factory installed on the memory board and provision is made to install additional 1 MB of memory, by using kit 3279-K???.

This description is in three parts:

- Part 1, **BUS BOARD CHECK** - This part describes how to check if the busboard installed in your computer will allow to install this kit or if a new busboard (3279-K$$$) must be installed first.

- Part 2, **BOARD PREPARATION** - This part describes the preparation of the boards and the function of the various straps on the boards of this kit.

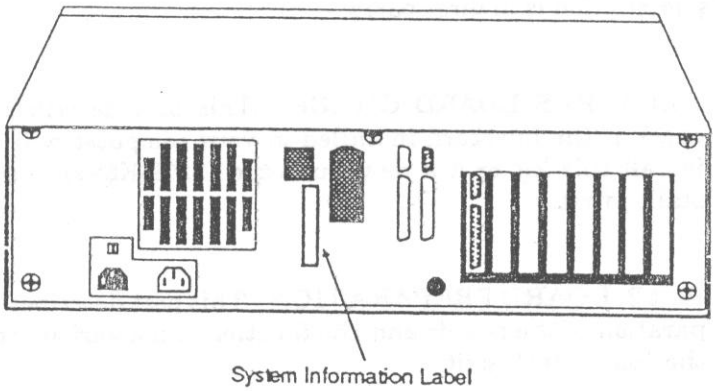
- Part 3, **INSTALLATION INFORMATION** - This provides the specific information needed to install the boards into your PC.

1. **Check your bus board, as described in the first part.**
2. **Read carefully the information in BOARD PREPARATION so that you understand how to prepare the boards.**
3. **Refer to the third part for the specific information for the installation of this kit to your PC.**

1 BUS BOARD CHECK

To check if the bus board installed in your computer allows the installation of this kit, use the following procedure:

1. Be sure that the power switch is off and remove the power cable from the PC. Make a note of their position and remove any peripheral cable from the PC.
2. Pull off the back cover and find the system information label on the back panel of the computer cabinet.



3. When number §§ on the label is marked with a cross, you can install the 80386 Upgrade kit.
4. When number @@ on the label is marked with a cross, the bus board must be replaced by a new style bus board (3279-K$$$) before the 80386 Upgrade kit can be installed. Refer to the documentation of 3279-K$$$ for information how to install the new bus board.
5. Do not forget to re-install the back cover and the previously removed cables before resuming computer operation after the bus board check.

2 BOARD PREPARATION

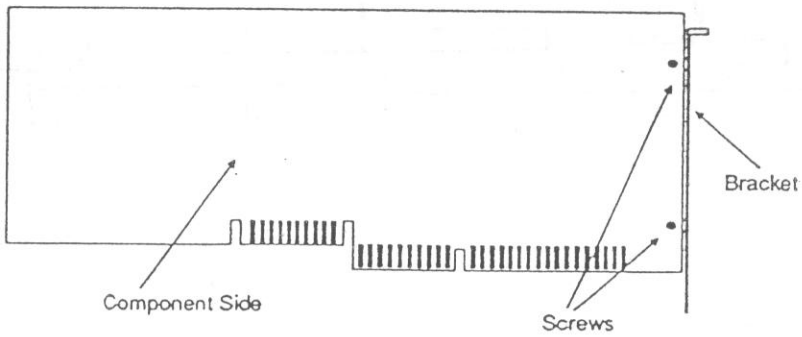
The boards could be damaged by electrostatic discharge once they have been removed from the packing. To avoid such problems, follow the recognised procedures for electrostatic discharge, such as:

- Always work in a static free area.
- Before handling the boards, discharge yourself by touching something that has a good connection to ground.
- Do not touch the components on the boards unless you are instructed to do so.
- Place the boards on an antistatic, padded surface when preparing the boards.

2.1 BRACKET INSTALLATION

To install the mounting brackets to the 80386 Processor Board and to the 80386 Memory Board use the following procedure:

- Align the tabs on the bracket with the holes provided on the right side of the board. Make sure the bracket is mounted on the solder side of the board as shown in the illustration.



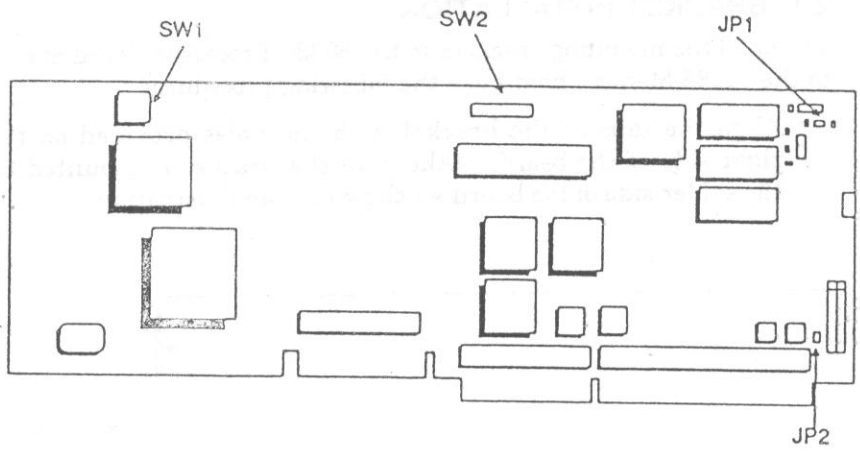
- Secure the bracket with the screws provided. Insert the screws from the component side of the board.

2.2 PROCESSOR BOARD 80386

2.2.1 Switches And Jumpers

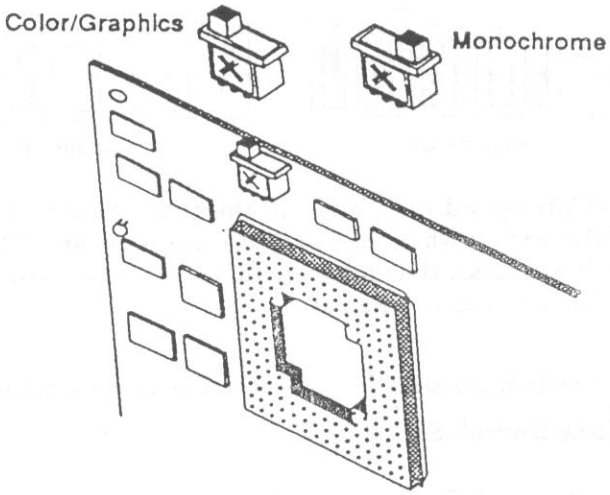
- It is necessary to set the switches and jumpers on the 80386 Processor Board.
  - The location of the jumpers and switches is shown in the illustration, their function is described below.
  - Jumpers are electrical bridges encapsulated in plastic to be placed onto connecting pins.

NOTE: The switch position marks engraved on the switches may differ from those used in this description: On = Closed, Off = Open



Switch Block SW1

The switch controls the type of display that is active.

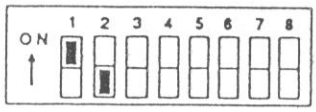


- Set switch SW 1 according to the video display to be used.

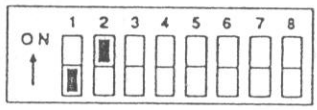
Switch Block SW2

The switch positions control several user selectable options:

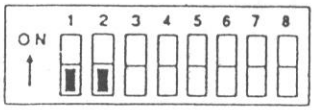
Coprocessor Switches SW2-1, SW2-2



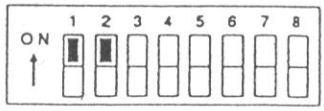
8038[illegible] Coprocessor Installed



80285 Coprocessor Installed

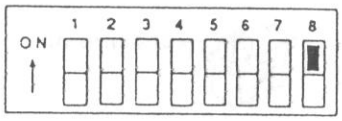


No Coprocessor Installed

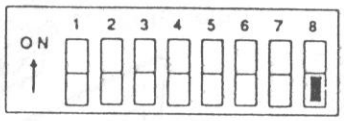


Invalid Setting

Processor Speed Switch SW2-8



High Speed

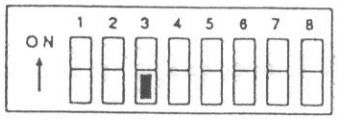


Automatic Speed

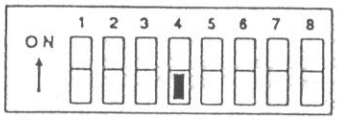
NOTE: High speed is 16 MHz all the time. Automatic speed is 16 MHz except when the flex disk is accessed and 8 MHz during flex disk access, thus allowing to load processor-speed dependent disk protection schemes.

The other switch positions of SW2 control factory-set options:

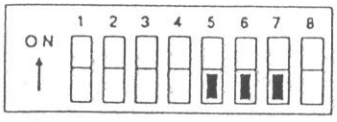
DMA Mode Switch SW2-3



Fail-Safe Interrupt Switch SW2-4



Interrupt Request Line Switches SW2-5, SW2-6. SW2-7



SW2 Setting

- Set the switches SW2-1 and SW2-2 for the type of co-processor installed.
- Set SW2-8 to select high or automatic processor speed.
- Check that the other switches of SW2 are correctly in the factory-set position as shown above.

Jumper JP1

- No jumper must be installed to the JP1 position.

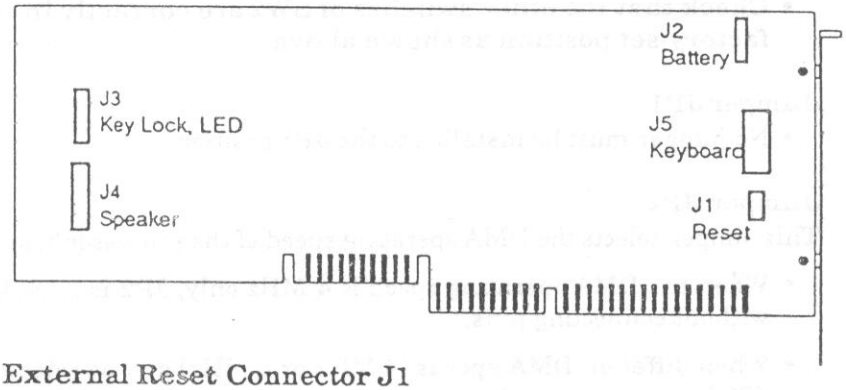
Jumper JP2

This jumper selects the DMA operating speed of the processor board.

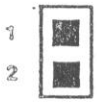
- When the DMA operating speed is 4 MHz only, JP2 is provided without connecting pins.
- When different DMA speeds (4 MHz or 8 MHz) can be selected, JP2 has connecting pins and the jumper is installed (8 MHz setting).

2.2.2 - Connector Data

The 80386 Processor Board has five external connectors. The locations are shown in the illustration and the pinouts of each connector are given in the figures that follow.

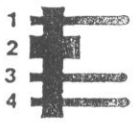


External Reset Connector J1



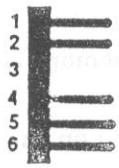
Pin	Description
1	Ground
2	Reset

Battery Backup Connector J2



Pin	Description
1	+ Voltage
2	Key
3	Power Good (active high)
4	Ground

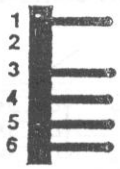
Keyboard Lock and Speed Indicator Connector J3



Pin	Description
1	LED "A" Power
2	Ground
3	key
4	+ Inhibit Keyboard
5	Ground
6	LED "B" Power

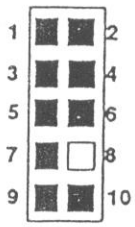
NOTE: Pin 6 can drive an LED to indicate high, 16 MHz, processor operation.
Pin 1 can drive an LED indicating any processor speed different from 16 MHz.
Grounding pin 4 will inhibit any input from the keyboard.

Speaker Connector J4



Pin	Description
1	Speaker Signal (- terminal)
2	Key
3	Ground
4	+ 5 Volts
5	Volume Control
6	Volume Control

Keyboard Connector J5

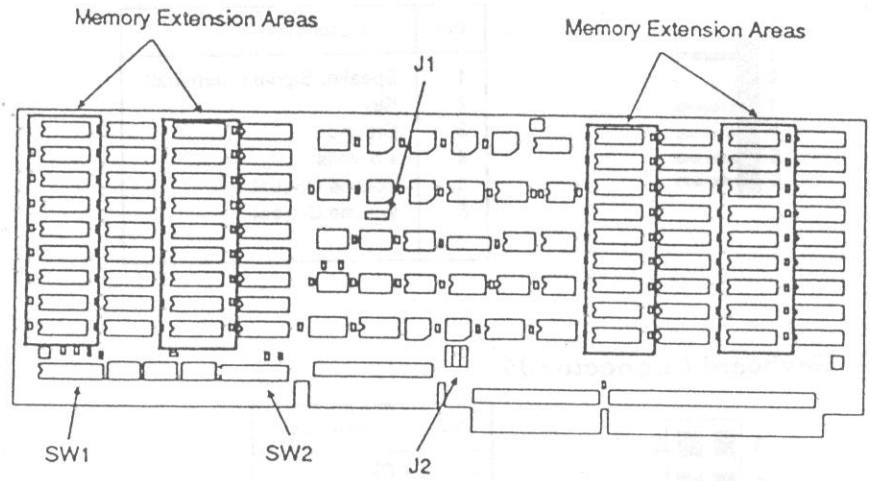


Pin	Description
1	+ Clock
2	Ground
3	+ Data
4	Ground
5	Power Good
6	Ground
7	+ 5 Volts
8	Key
9	Ground
10	Ground

2.3 MEMORY BOARD 80386

- If you are increasing the capacity of the memory board by adding kit 3279-K???, the additional ICs should be added to the areas shown in the illustration.
  - The method of installing the additional memory is given in the kit information of kit 3279-K???.
- It is necessary to set the switches and jumpers on the Memory Board.
  - The location of the jumpers and switches is shown in the illustration, their function is described below.
  - Jumpers are electrical bridges encapsulated in plastic to be placed onto connecting pins.

NOTE: The switch position marks engraved on the switches may differ from those used in this description: On = Closed, Off = Open

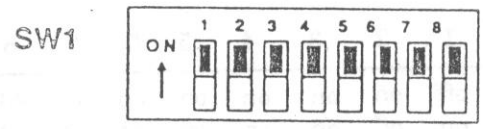


2.3.1 SWITCHES AND JUMPERS

Switchblock SW1

- Switches 1 through 7 on switchblock SW1 control the assigned location of the memory
- Switch 8 identifies the first megabyte of memory in the system.
- Switchblock SW1 on this board must always be set for the first 2 MB boundary as shown in the illustration.

  NOTE: Setting of SW1 is the same for the basic 1 MB board and the board upgraded to 2 MB.



- **Check that all switches of SW1 are set to the ON position.**

Switchblock SW2

- SW2 positions 256 KB of video display and expansion ROM from the first megabyte of memory to the end of the installed memory (in 1 MB increments).
- Since the 80386 Memory Board may not be the only memory board to be installed, it is not possible to provide fixed switch settings of SW2 on this board.
- Refer to the table below for the switch setting - the MEMORY BOARD SWITCH SETTING EXAMPLES at the end of this chapter provide additional elucidation.

Total System Memory	Switch SW2							
	1	2	3	4	5	6	7	8
1.0MB	off	on	on	on	on	on	on	on
2.0MB	on	off	on	on	on	on	on	on
3.0MB	off	off	on	on	on	on	on	on
4.0MB	on	on	off	on	on	on	on	on
5.0MB	off	on	off	on	on	on	on	on
6.0MB	on	off	off	on	on	on	on	on
7.0MB	off	off	off	on	on	on	on	on
8.0MB	on	on	on	off	on	on	on	on
9.0MB	off	on	on	off	on	on	on	on
10.0MB	on	off	on	off	on	on	on	on
11.0MB	off	off	on	off	on	on	on	on
12.0MB	on	on	off	off	on	on	on	on
13.0MB	off	on	off	off	on	on	on	on
14.0MB	on	off	off	off	on	on	on	on
15.0MB	off	off	off	off	on	on	on	on

On = Closed Off = Open

- Set SW2 according to the amount of memory installed in your computer.

Jumper J1

J1 controls the RAM chip speed. The F on the left side of the jumper is next to pin 1.

- pins 1 and 2 connected ⇔ 70 nanoseconds memory speed
- pins 2 and 3 connected ⇔ 120 nanoseconds memory speed

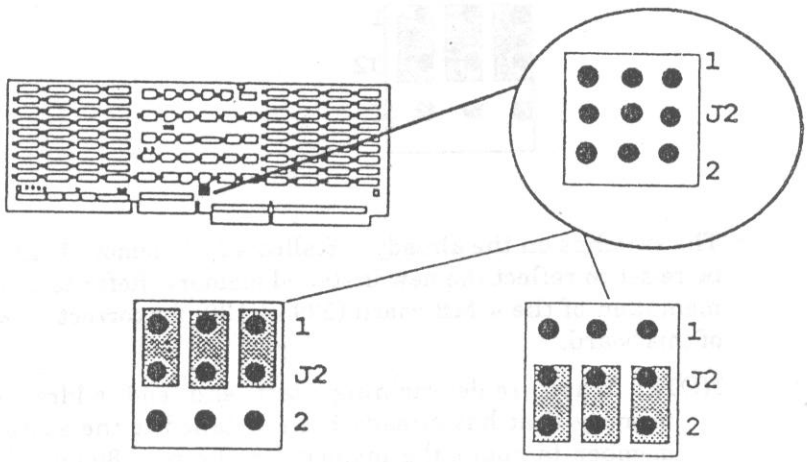
NOTE: The jumper is factory-set for 70 nanoseconds memory speed.

- The memory chips on the board allow 120 nanoseconds memory speed.
- Memory boards with either 70- or 120-nanosecond chips can be used, but if they are mixed they must all be used at the slower speed.

- **Set the jumper to determine the desired memory speed.**

Jumper J2

J2 controls the amount of active memory on the board.



1 MB On-board Memory 2 MB On-board Memory

- **Set the jumpers according to the amount of actual on-board memory.**

NOTE: Factory installed memory is 1 MB; upgrade to 2 MB is provided with kit 3279-K???

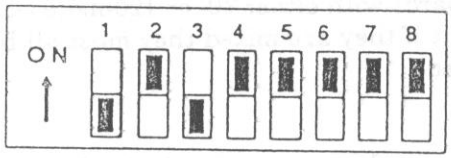
2.3.2 MEMORY BOARD SWITCH SETTING EXAMPLES

Example 1

Your system has a memory extension board with 4 MB memory (3299-K130 + 7 kits 3299-K131) already installed and you are about to install this kit (with 1 MB memory board).

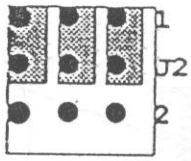
SW1 setting: all switches ON

SW2 setting:(total system memory: 5 MB)



Jumper J1: pins 1 and 2 connected (70 nanosecond setting)

Jumper J2: (1 MB on-board memory)



- The switches on the already installed 4 MB memory board must be re-set to reflect the new installed memory. Refer to the documentation of the 4 MB board (3299-K130) for correct strapping of this board.

  NOTE: When re-determining start and end addresses for memory that has already been installed to the system, remember to count the memory on the new 80386 Memory Board as 'already installed additional memory'.

Example 2

There is no additional memory board installed to your system and you are about to install this kit with the Memory Board upgraded to 2 MB of memory capacity (3279-K010 + 3279-K???).

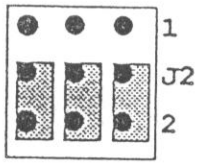
SW1 setting: all switches "ON"

SW2 setting:(total system memory: 2 MB)

Jumper J1:

- pins 1 and 2 connected (70 nanosecond setting) or
- pins 2 and 3 connected (120 nanosecond setting)

Jumper J2: (2 MB on-board memory)



3 INSTALLATION INFORMATION

This section contains the information necessary to install the kit into the following PCs
:

- 3279

3.1 3279 INSTALLATION

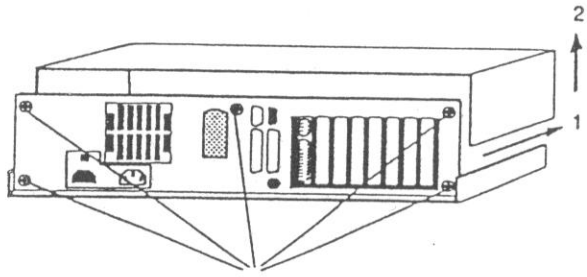
Installation of this kit consists of replacing the existing main processor board by the 80386 Processor Board and the additional installation of the 80386 Memory Board in the adjacent bus slot. The installation of the 80386 boards requires the 32 bit extender bus board.

CAUTION

If there is a hard disk drive installed in your computer, make sure to park the hard disk (type in PARK in response to the MS-DOS prompt) before starting any installation on the computer

1. **Remove the cables.**
   - Be sure that the power switch is off and remove the power cable from the PC.
   - Make a note of their position and remove any peripheral cable from the PC.

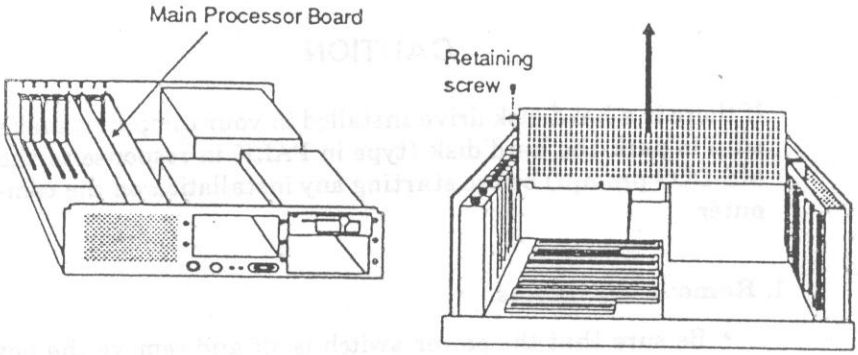
2. **Remove the cabinet top.**
   - Pull off the back cover, remove the five cabinet retaining screws as shown in the illustration.
   - Slide the cabinet top forward slightly and lift it off.



Retaining Screws

3. **Remove the Main Processor Board**

- Locate the Main Processor Board (normally this is in slot 6, the third slot counted from the power supply),
- Remove the retaining screw and carefully remove the Main Processor Board as shown in the illustration - make sure not to break any cable that is connected to the board.



- Make a note of their positions (e.g. note the "J" number of the board connector where the cable is connected to) and disconnect all the cables from the Main Processor Board.

4. **Remove any board from slot 5.**

- Using the same procedure, remove any board that may be installed in slot 5.

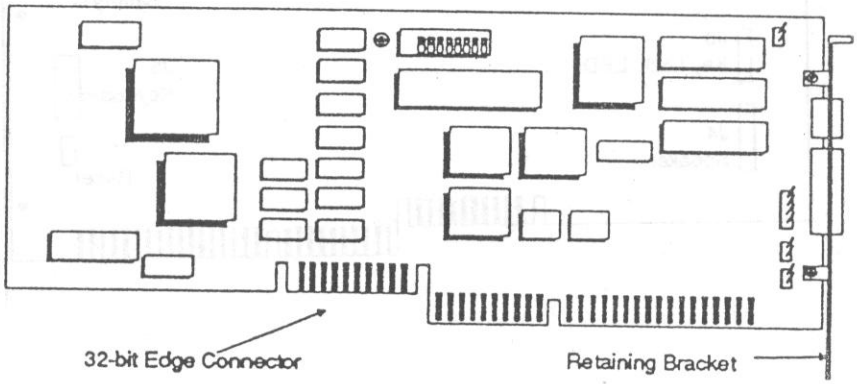
NOTE: For future use this board must be installed in a different empty slot as slot 5 will be occupied by the 80386 Memory Board.

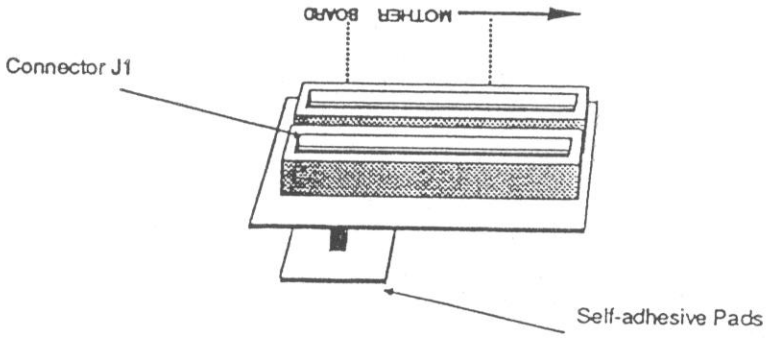
5. **Check the strapping of the 80386 boards.**

   - Carefully check that all strapping on the 80386 Processor Board and on the 80386 Memory Board has been carried out as described in **BOARD PREPARATION**

6. **Connect the 32 bit extender bus board.**

   - Identify the message "<------- MOTHER BOARD" and connector J1 on the 32 bit extender bus board
   - Plug connector J1 of the bus extender board to the 32 bit edge connector on the 80386 Processor Board - make sure that the "Mother Board" arrow points to the retaining bracket on the solder side of the processor board. (Refer to the illustration)

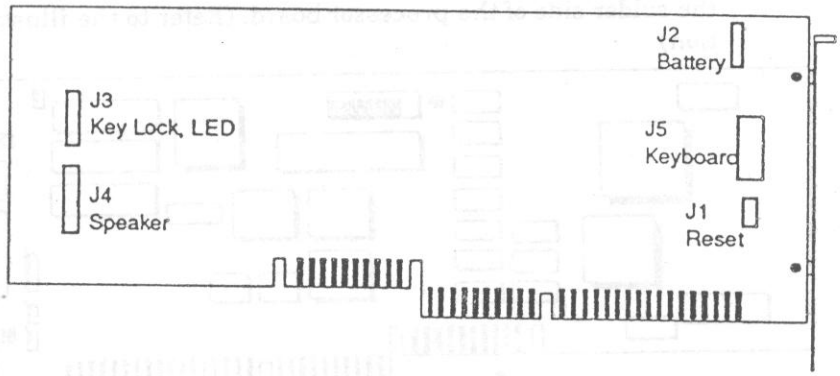




   - Remove the protective film from the self-adhesive pads on the plastic feet of the extender bus board

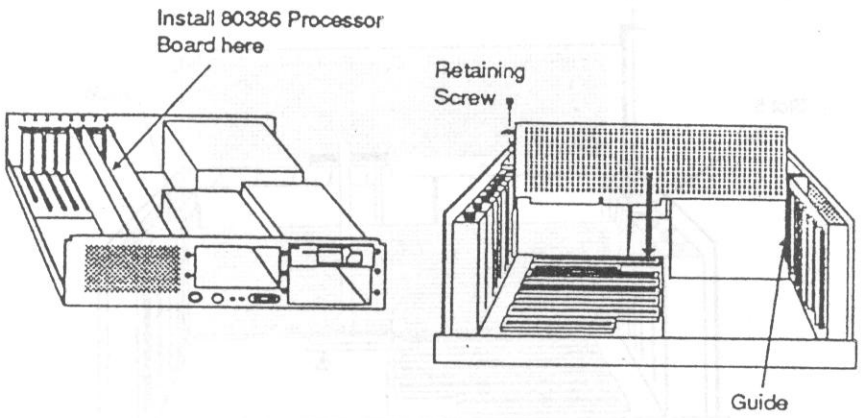
7. Connect the cables to the 80386 Processor Board

- The cables removed from the old main processor board must be connected to the same position on the 80386 Processor Board
- Connect the
  battery cable to connector **J2**
  keylock cable to connector **J3**
  speaker cable to connector **J4**
  keyboard cable to connector **J5**
  on the 80386 Processor Board
- The connectors are keyed to prevent wrong connection.



8. **Install the 80386 Processor Board (+ extender bus board)**

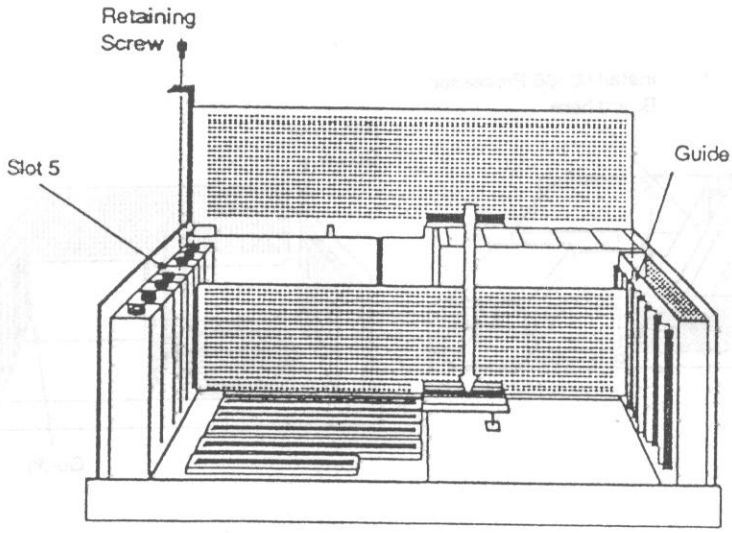
- Place the 80386 processor board with the extender bus board attached in slot 6. The empty slot on the extender bus board should coincide with slot 5.
- Make sure that the edge connectors engage properly in the sockets of the bus board, then press the processor board firmly into place.
- The longer plastic stand-off of the Bus Extender Board should rest on the cabinet base.
- Ensure also that the edge of the board nearest the loud-speaker drops into the plastic guide.



- Use the screw which previously held the old Main Processor Board in place to fasten the bracket attached to the 80386 Processor Board.

9. **Install the 80386 Memory Board.**

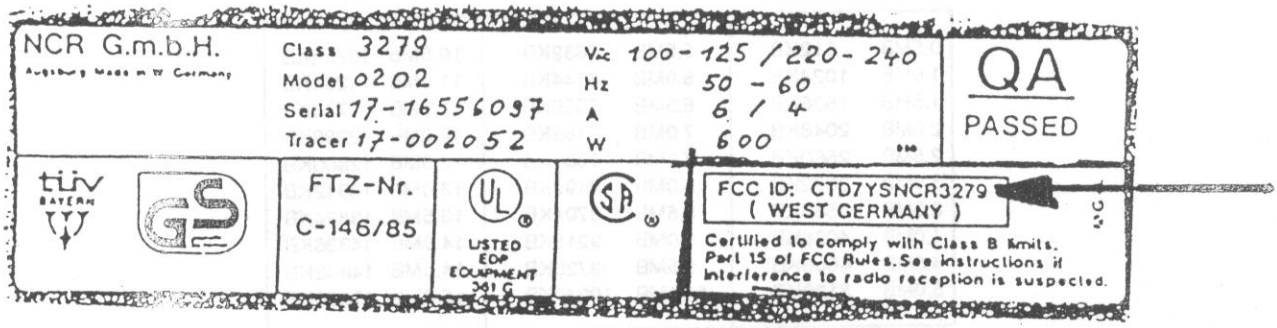
- Remove the blanking plate for slot 5, if there was no board installed in the slot before. The blanking plate is held in place by a single screw.
- Plug the 80386 Memory Board into slot 5 facing upward from the bus board.
- Make sure that the edge connectors engage properly in the sockets of the bus board and the bus extender board, then press the board firmly into place.
- Ensure that the edge of the board nearest the loudspeaker drops into the plastic guide.



- Use the screw which previously held the blanking plate (or another board) in place to fasten the bracket attached to the 80386 Memory Board.

10. Re-assemble the computer.

- Re-install the cabinet top,
- Find the name-plate label on the rear side of the cabinet. Paste the Label "FCC ID:" provided with the kit over the corresponding section of the name-plate label.



- Re-install the back cover.
- connect the previously removed peripheral cables. Re-connect the power cable.

11. Run HARDWARE-SETUP

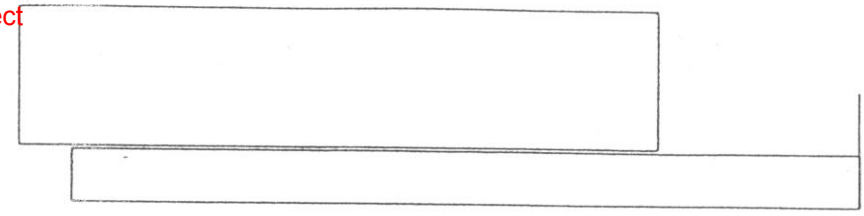
- Run HARDWARE-SETUP (as described in your Owner's Manual) to declare the new installed features to the system. You are required to enter the memory size in kilobytes - the following table will help you to convert megabytes (MB) to kilobytes (kB).

0.5MB	512KB	5.5MB	5632KB	10.5MB	10752KB
1.0MB	1024KB	6.0MB	6144KB	11.0MB	11264KB
1.5MB	1536KB	6.5MB	6656KB	11.5MB	11776KB
2.0MB	2048KB	7.0MB	7168KB	12.0MB	12288KB
2.5MB	2560KB	7.5MB	7680KB	12.5MB	12800KB
3.0MB	3072KB	8.0MB	8192KB	13.0MB	13312KB
3.5MB	3584KB	8.5MB	8704KB	13.5MB	13824KB
4.0MB	4096KB	9.0MB	9216KB	14.0MB	14336KB
4.5MB	4608KB	9.5MB	9728KB	14.5MB	14848KB
5.0MB	5120KB	10.0MB	10240KB	15.0MB	15360KB

Your PC is now ready for use.

3.2 DIAGNOSTICS

- Inpredictable errors may be falsely indicated by the USER DIAGNOSTICS provided with your computer when used with an 80386 Processor system.
- Only the **USER DIAGNOSTICS diskette provided with this kit** should be used when running diagnostics with the 80386 Upgrade kit installed to your system.



NCR

Personal Computer Division

Doc.: 017-0038184

Main Processor Board Logic Diagram

U NUMBER	PIN NUMBERS +5	GND	UNUSED
1	16	8	
2	20	10	
3	10,14	7	
4	14	7	
5	20	10	
6	24	1,2,12	
7	20	10	
8	20	10	
9		35	
10	1,28	14	
11	16	8	
12	16	8	
13	20	10	
14	***	***	
15	20	10	
16	24	1,2,12	
17	14	7	
18	2,4,10,13,14	7	
19	14	7	
20	16	8	
21	14	7	
22	20	10	
23	24	1,2,12	
24	14	7	
25	2,10,13,14	7	
26	14	7	
27	illegible	illegible	
28	1,28	14	
29	20	10	
30	20	10	
31	20	10	
32	20	10	
33	14	7	
34	5	6,7,10	
35	14	7	
36	14	7	

U NUMBER	PIN NUMBERS +5	GND	UNUSED
37	2,3,4,6,14	7,11	
38	14	7	
39	20	10	
40	13,17,28	14	
41	20	10	
42	20	10	
43	20	10	
44	28	14	
45	2,4,10,14	7	
46	2,4,10,13,14	7	
47	***	***	
48	20	10	
49	7,34	22,23	
50	7,34	23	
51	16	8	
52	20	10	
53	20	10	
54	2,3,13,14	7	
55	20	10	
56	1,16	8	
57	20	10	
58	5,6,16	8	
59	20	10	
60	20	10,11	
61	14,16	8,15	
62	14	7	
63	14	7	
64	20	10,19	
65	16	8	
66			
67	20	1,10	
68	1,16	8	
69			
70	20	10	
71	20	10	
72	20	10	

U NUMBER	PIN NUMBERS +5	GND	UNUSED
73	20	10	
74	20	10	
75	31,44	14,22	
76	16,28	14	
77	28	14,16	
78	20	10,19	
79	16	8,12	
80	14	7	
81	16	8	
82			
83	20	1,10	
84	20	10	
85	20	10	
86	16	8	
87	20	10	
88	20	10,11	
89			
90			
91			
92			
93			
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99			
100			
101			
102			
103			
104			
105			
106			
107			
108			

U NUMBER	PIN NUMBERS +5	GND	UNUSED
109			
110			
111			
112			
113			
114			
115			
116			
117			
118			
119			
120			
121			
122			
123			
124			
125			
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132			
133			
134			
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136			
137			
138			
139			
140			
141			
142			
143			
144			

U NUMBER	PIN NUMBERS +5	GND	UNUSED
145			
146			
147			
148			
149			
150			
151			
152			
153			
154			
155			
156			
157			
158			
159			
160			
161			
162			
163			
164			
165			
166			
167			
168			
169	11,13,14	7	
170			
171			
172			
173			
174			
175			
176			
177			
178			
179			
180			
181			
182	20	10	

***

U14 +5V PINS: B7,B10,C1,C5,D13,F2 G2,G11,K1,K3,K12 L6,L13,M5,M8 N3,N10

GND PINS: A1,A5,A10,C3,C8,D12 F3,G3,G12,K2,K11, L12,M6,N4,N13 ,N8

***

U47 +5V PINS: A1,A5,A7,A10,A14,C5,C12,D12,F13 G2,G3,G12,G14,L12,M3,M7,M13 N4,N7,P2,P8

GND PINS: A2,A6,A9,B1,B5,B11,B14,C11,F2,F3, F14,J2,J3,J12,J13,M4,M8,M10 N3,P6,P14

Figure 7-1 Main Processor Board
(1 of 20)

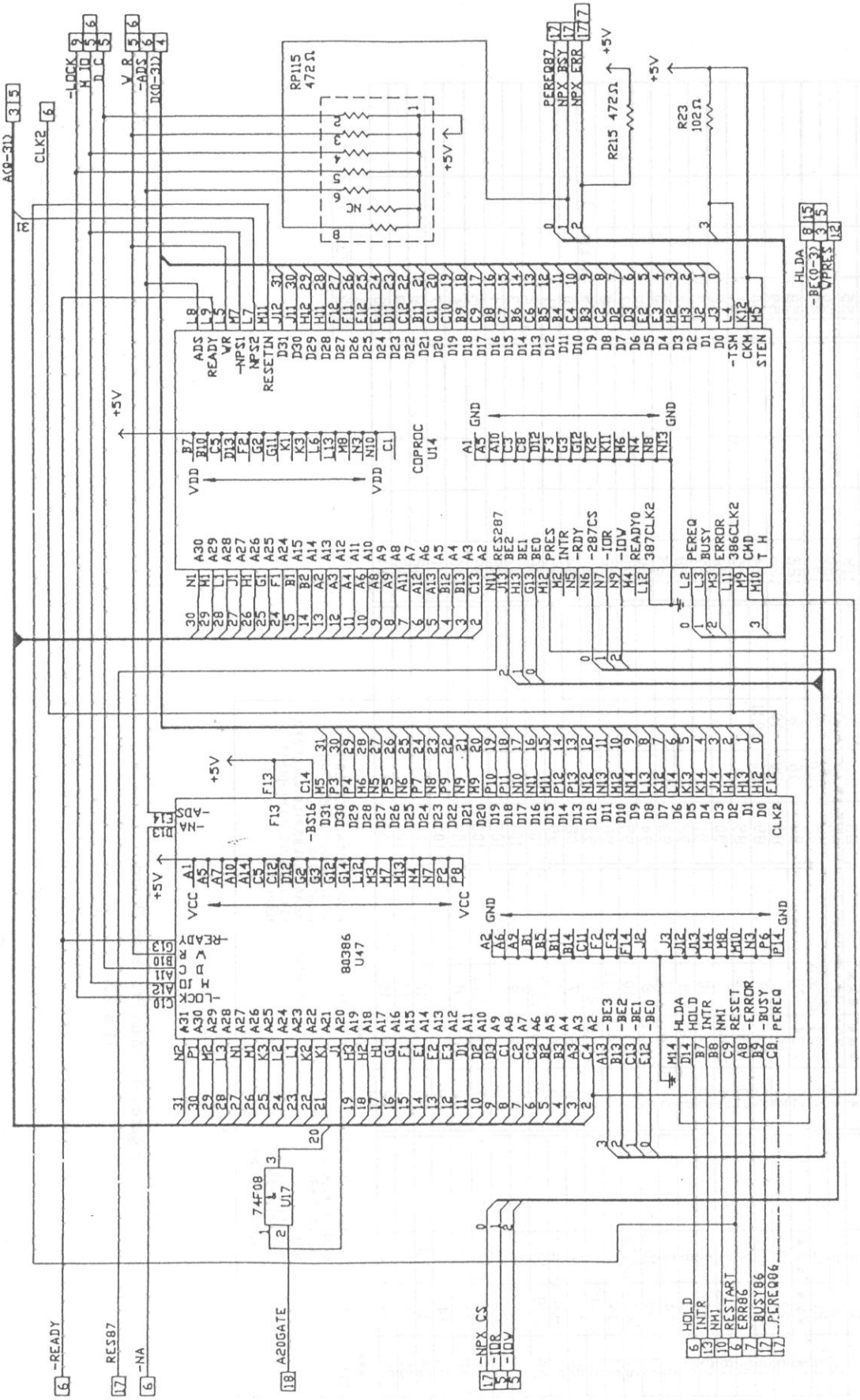

Figure 7-1 Main Processor Board
(2 of 20)

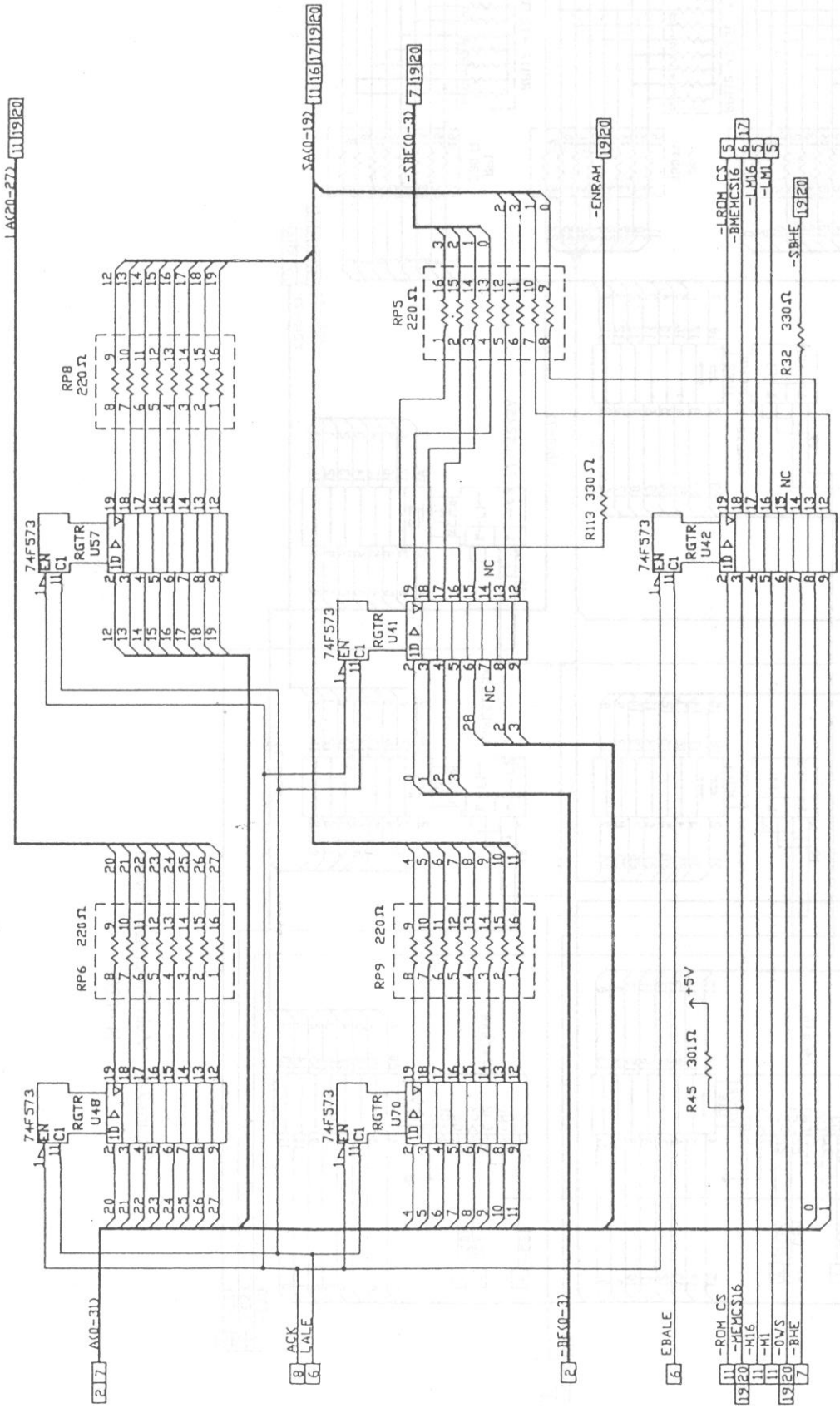

Figure 7-1 Main Processor Board
(3 of 20)

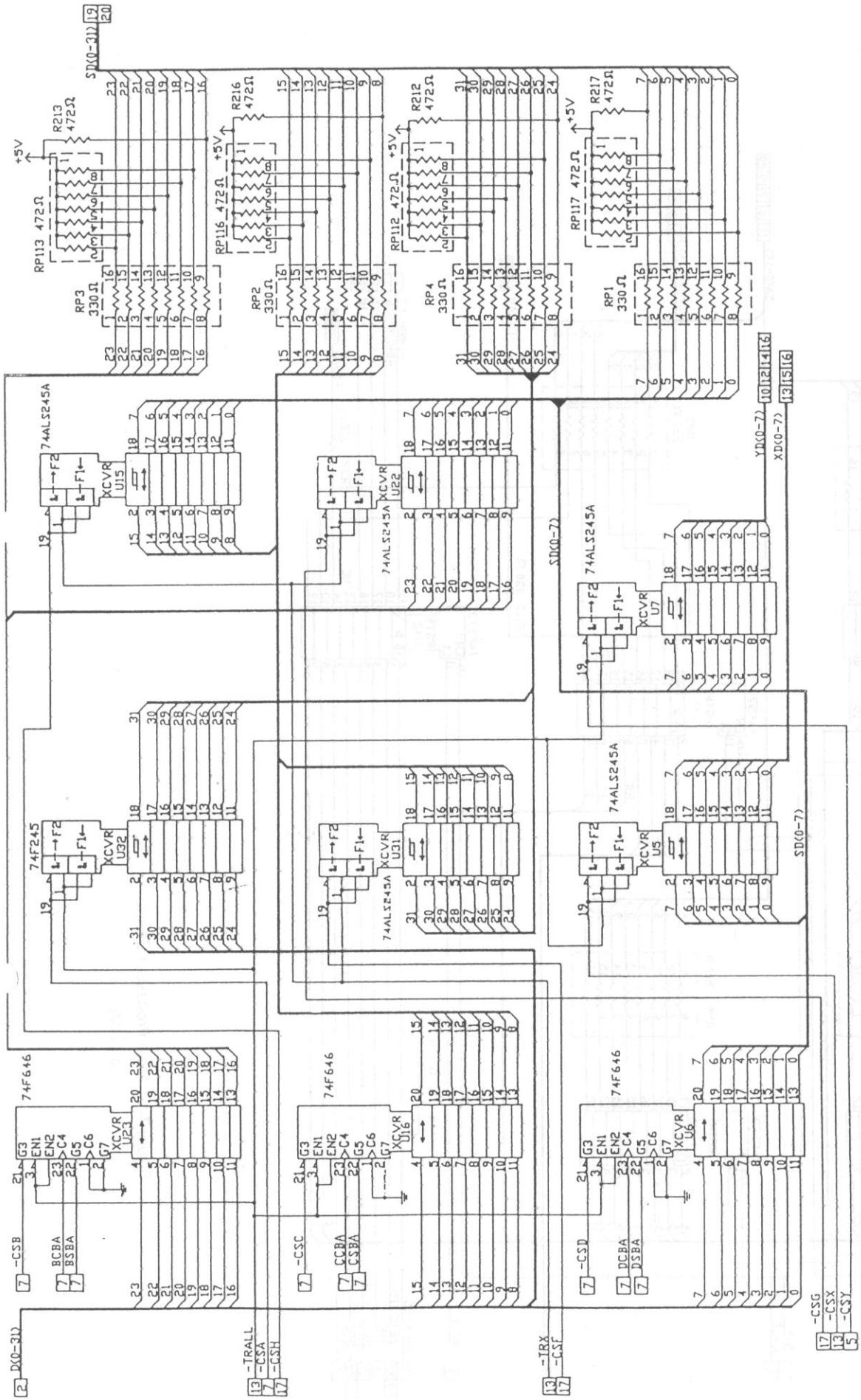

Figure 7-1 Main Processor Board
(4 of 20)

LOGIC DIAGRAMS

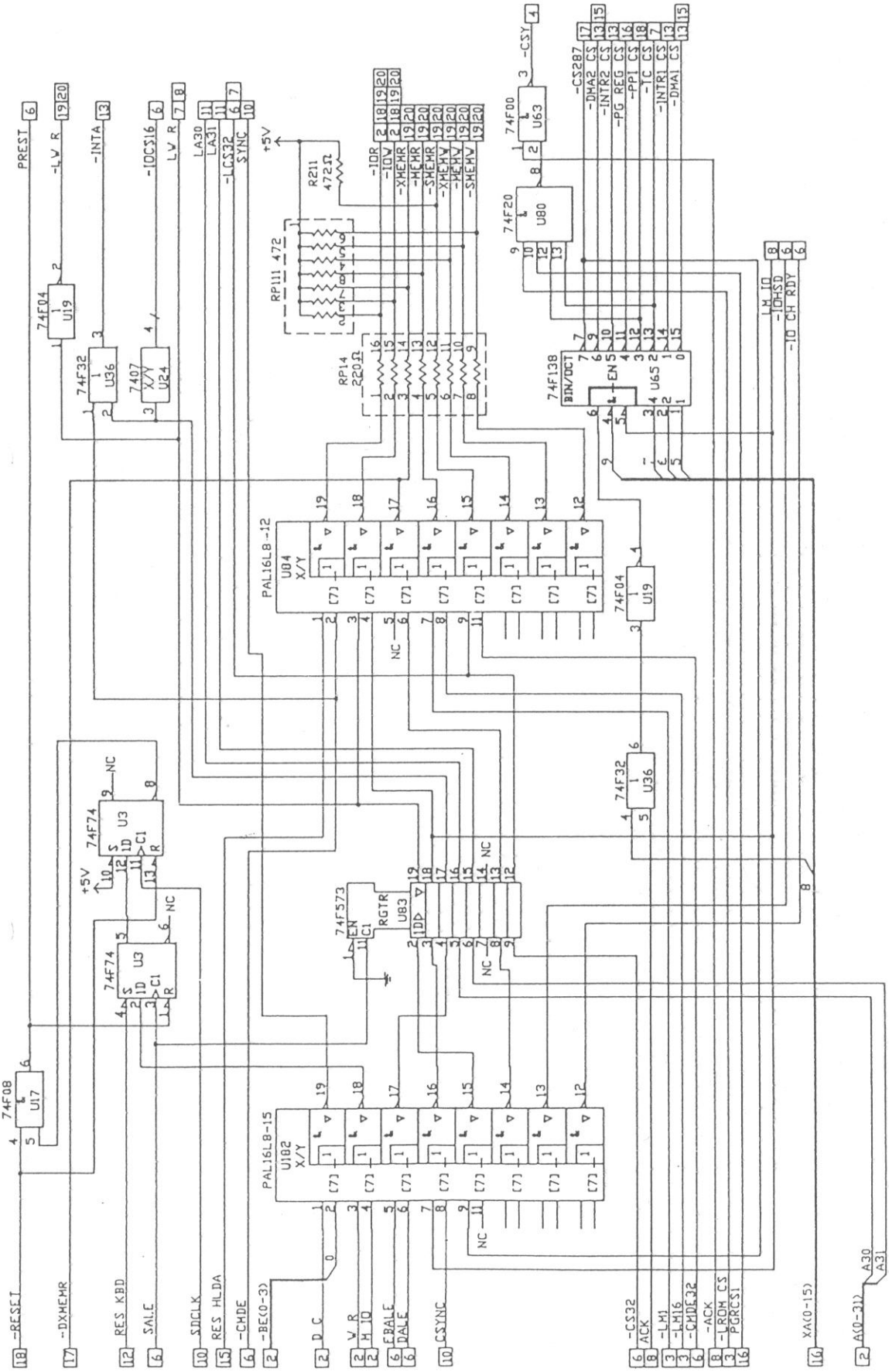

Figure 7-1 Main Processor Board
(5 of 20)

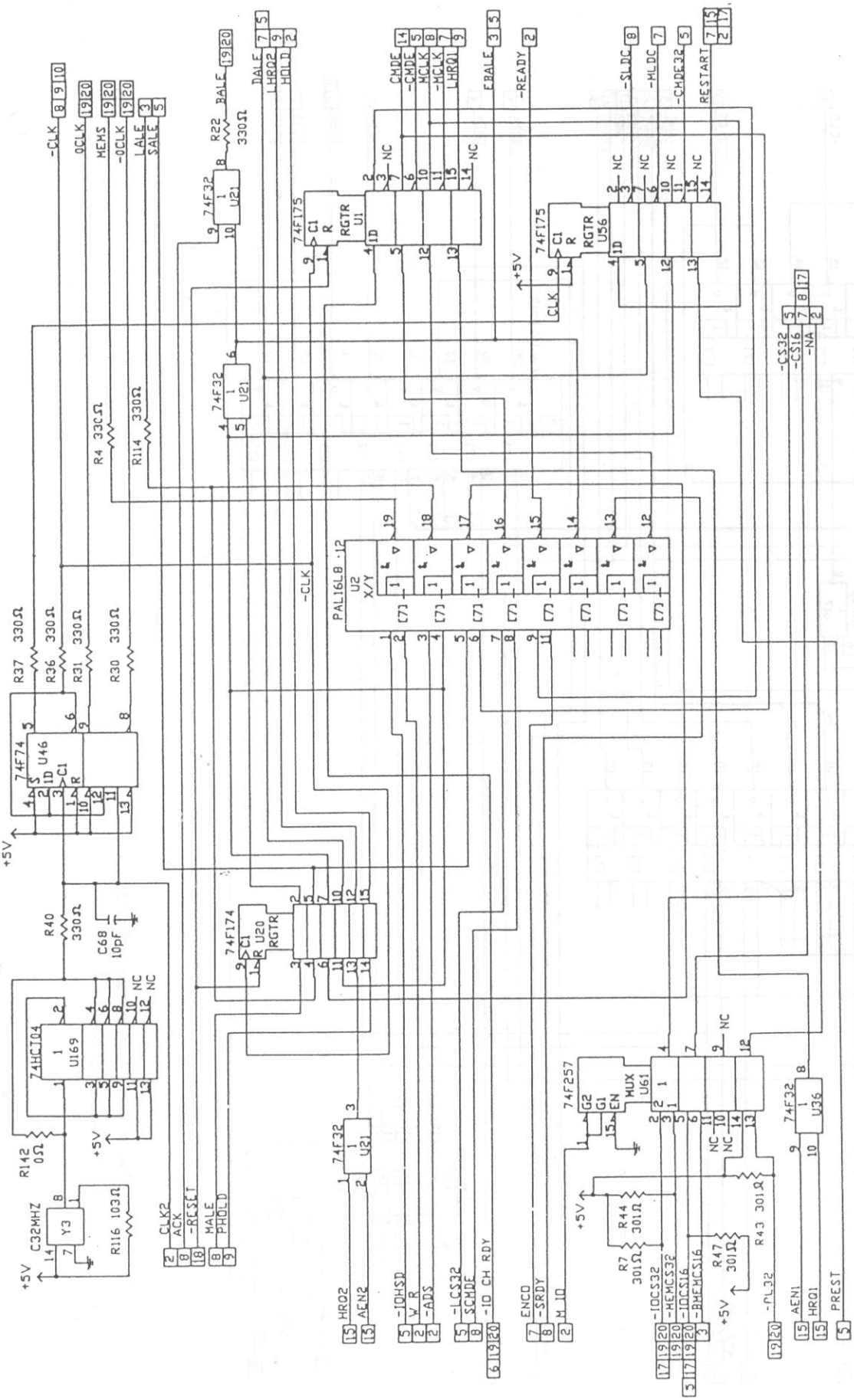

Figure 7-1 Main Processor Board
(6 of 20)

LOGIC DIAGRAM

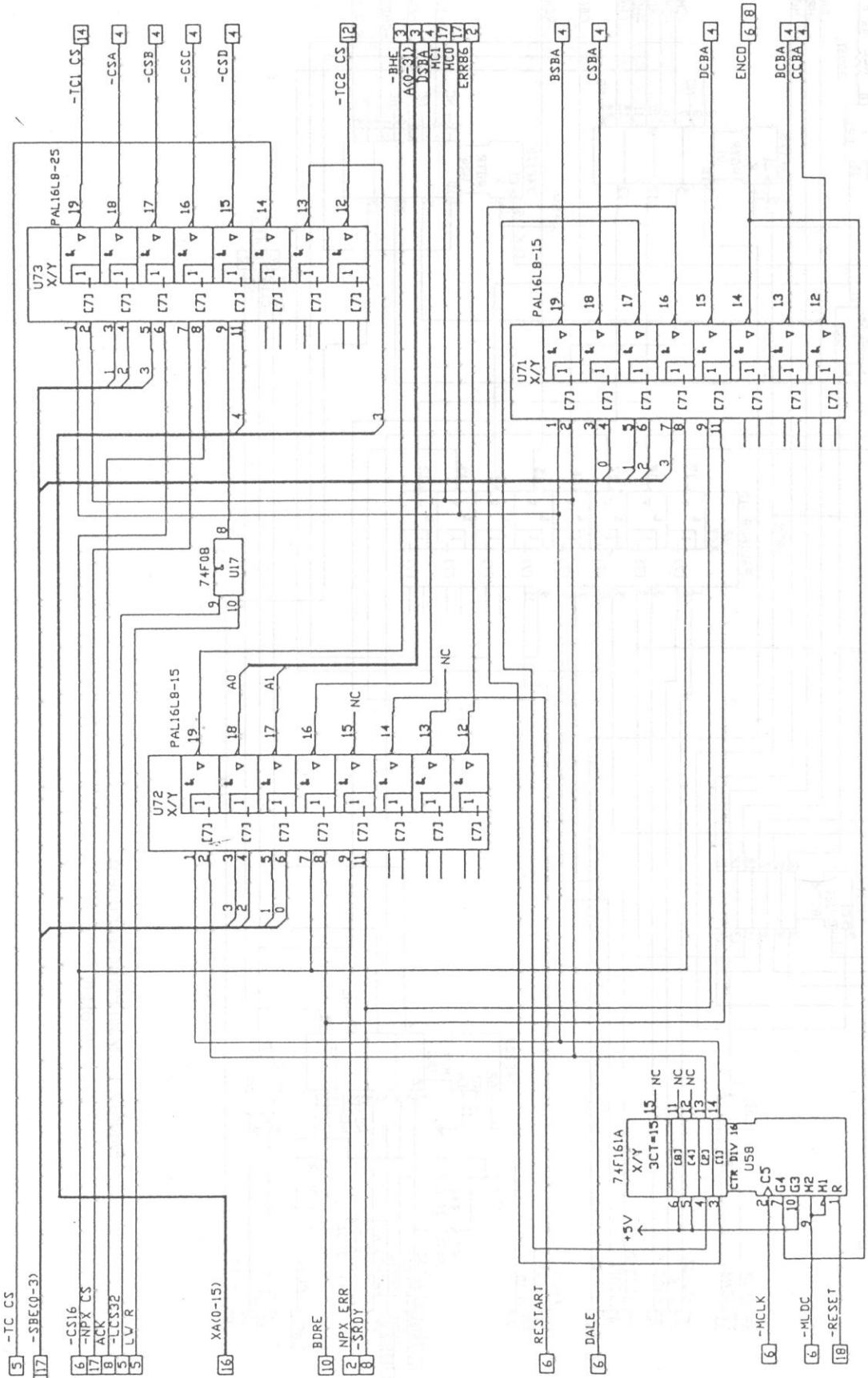

Figure 7-1 Main Processor Board
(7 of 20)

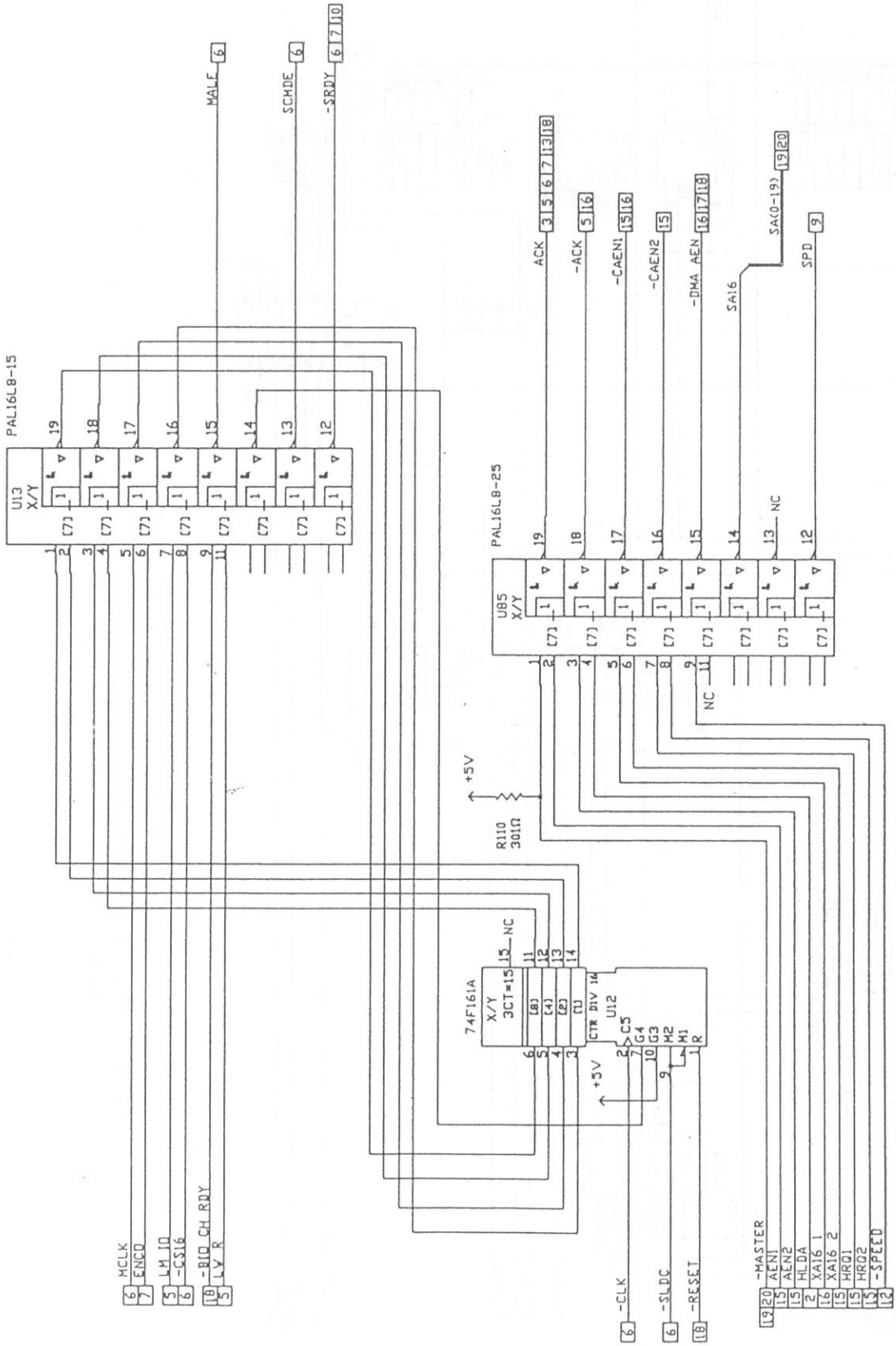

Figure 7-1 Main Processor Board
(8 of 20)

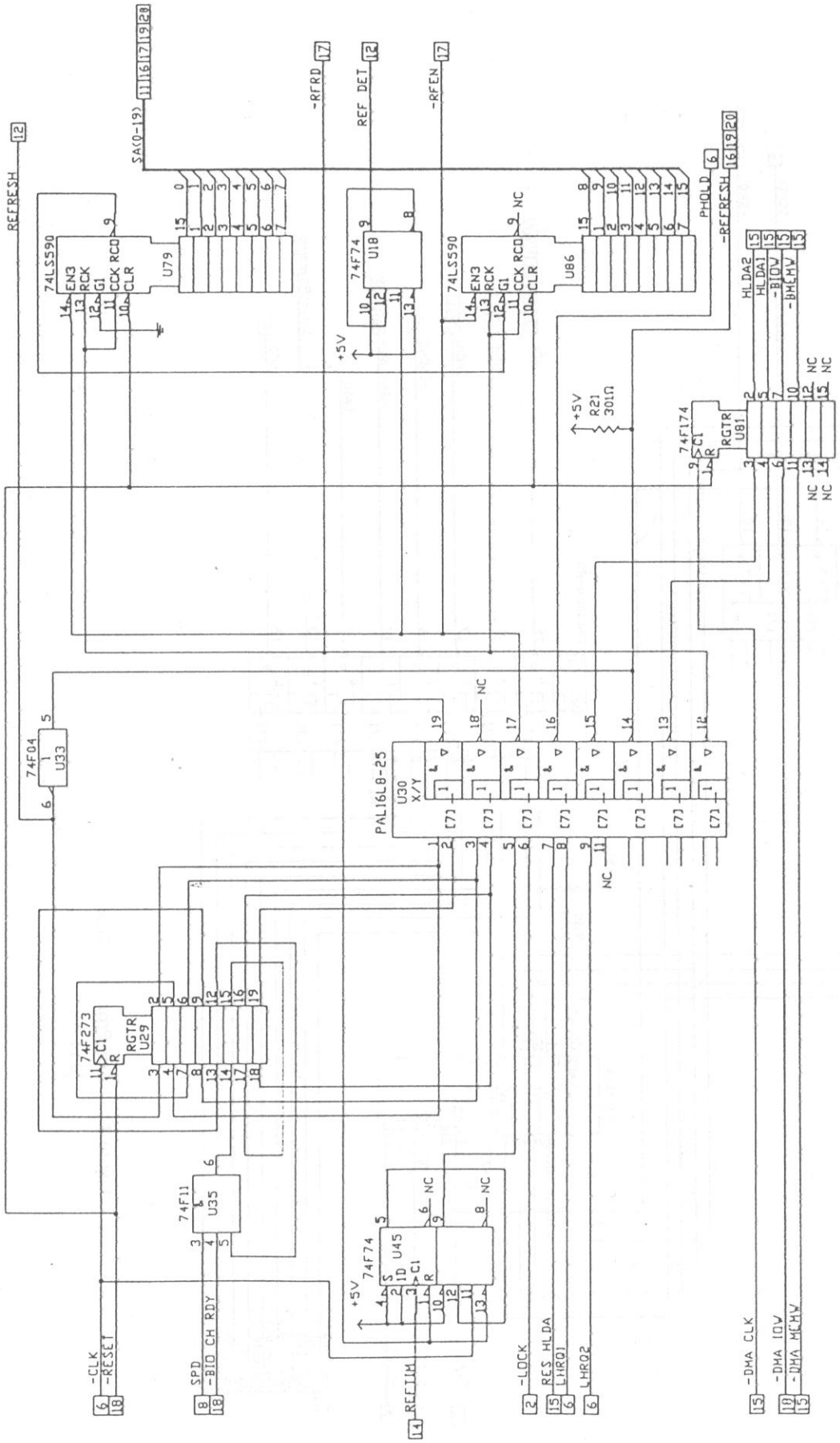

Figure 7-1 Main Processor Board
(9 of 20)

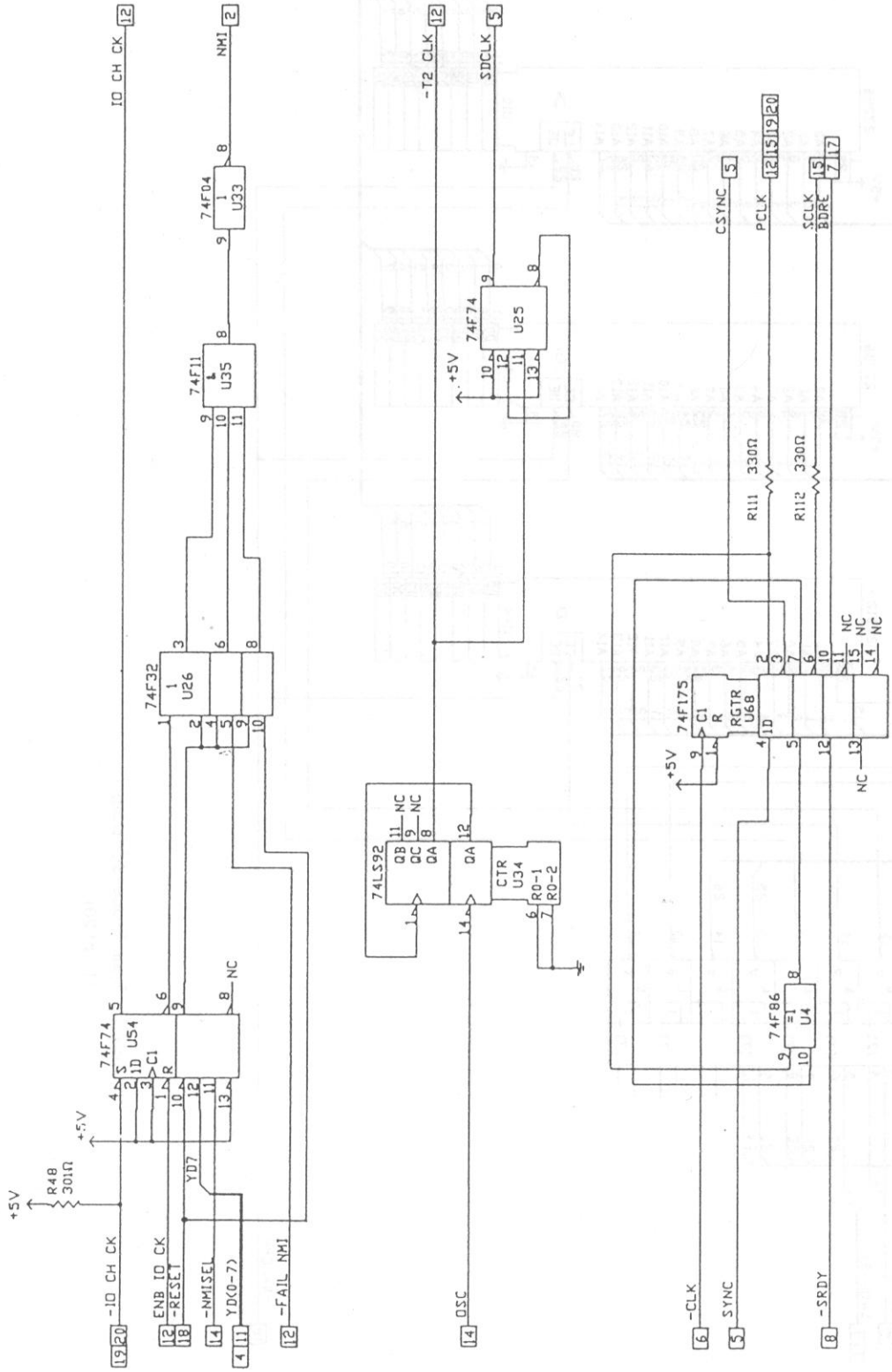

Figure 7-1 Main Processor Board
(10 of 20)

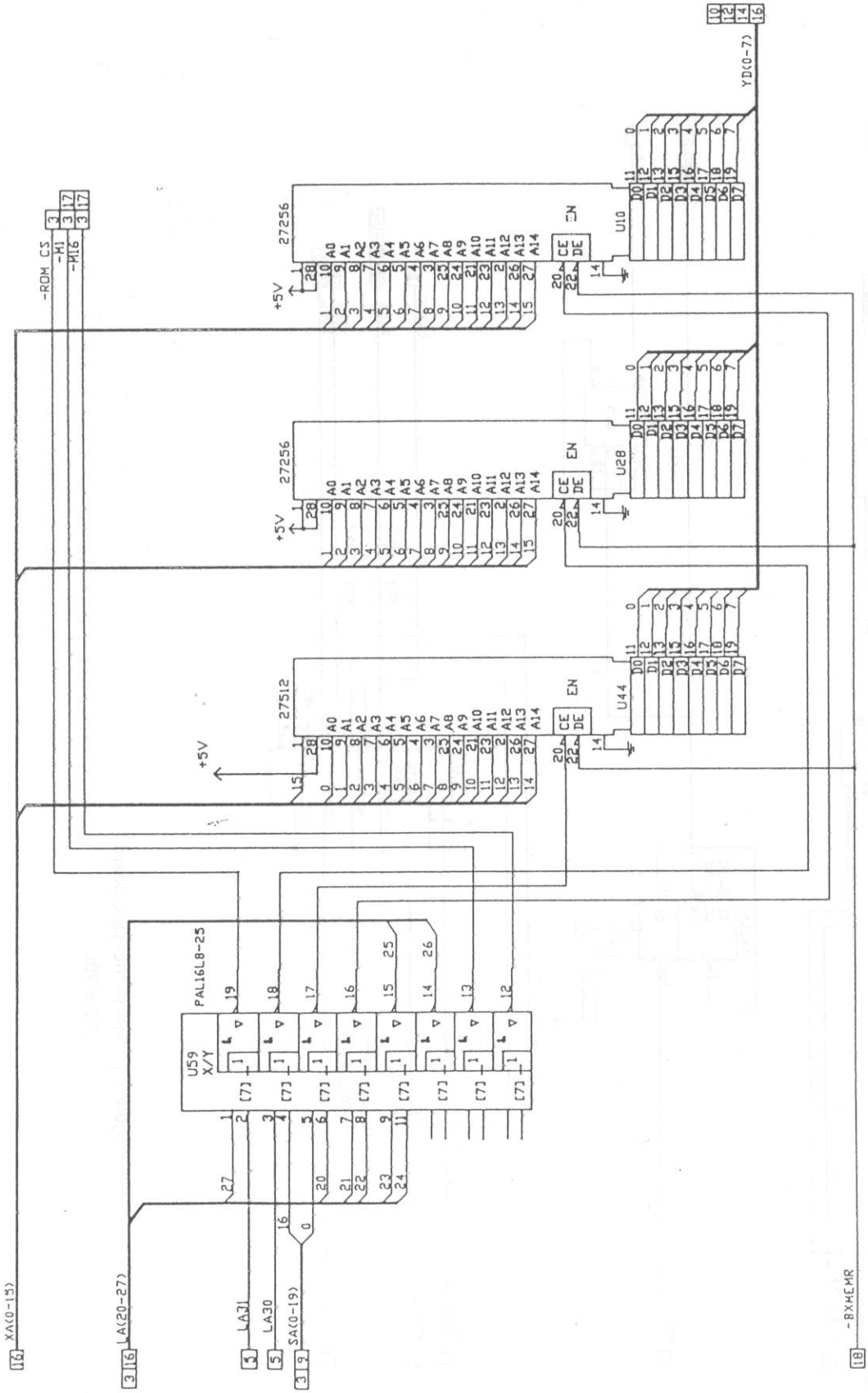

Figure 7-1 Main Processor Board
(11 of 20)

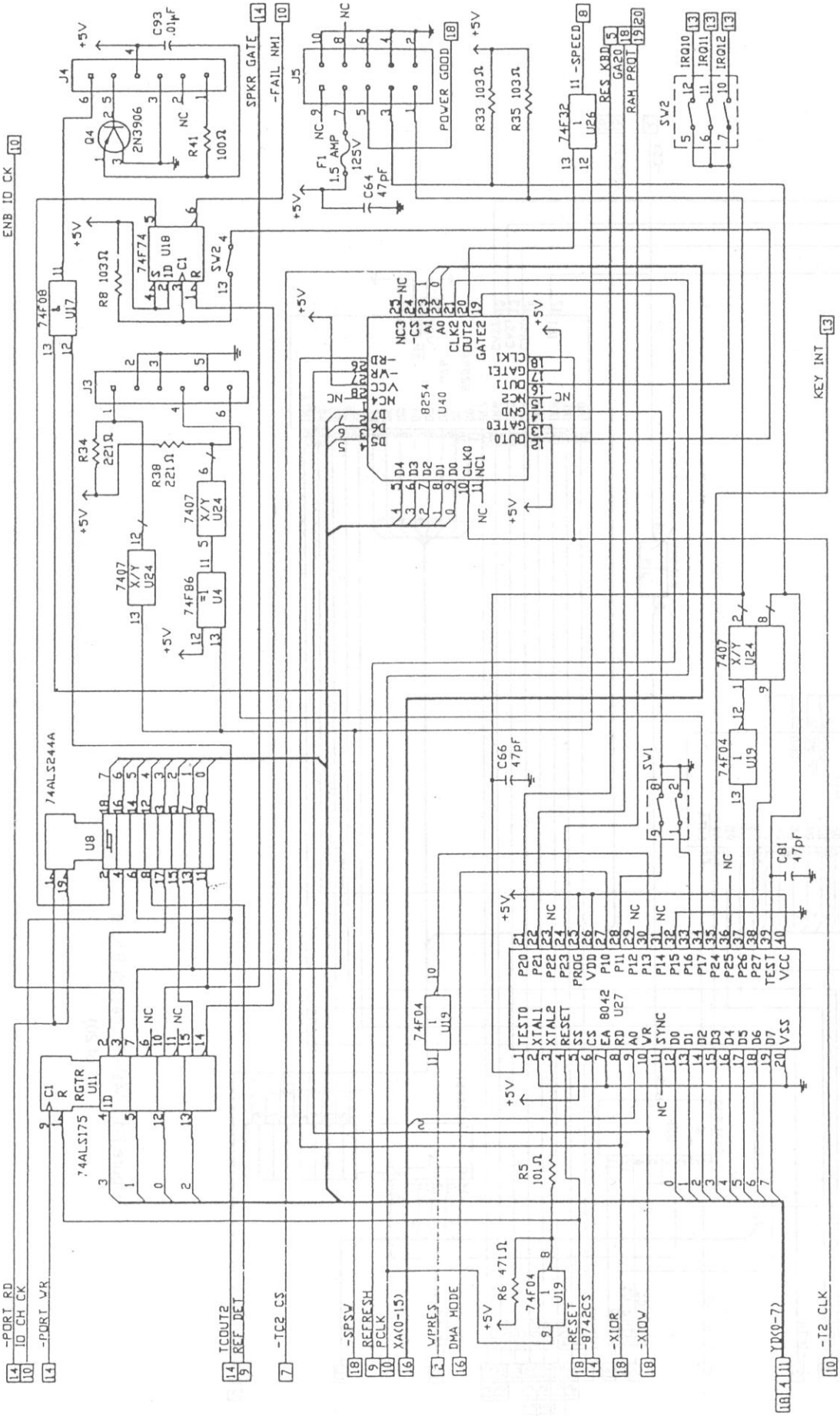

Figure 7-1 Main Processor Board
(12 of 20)

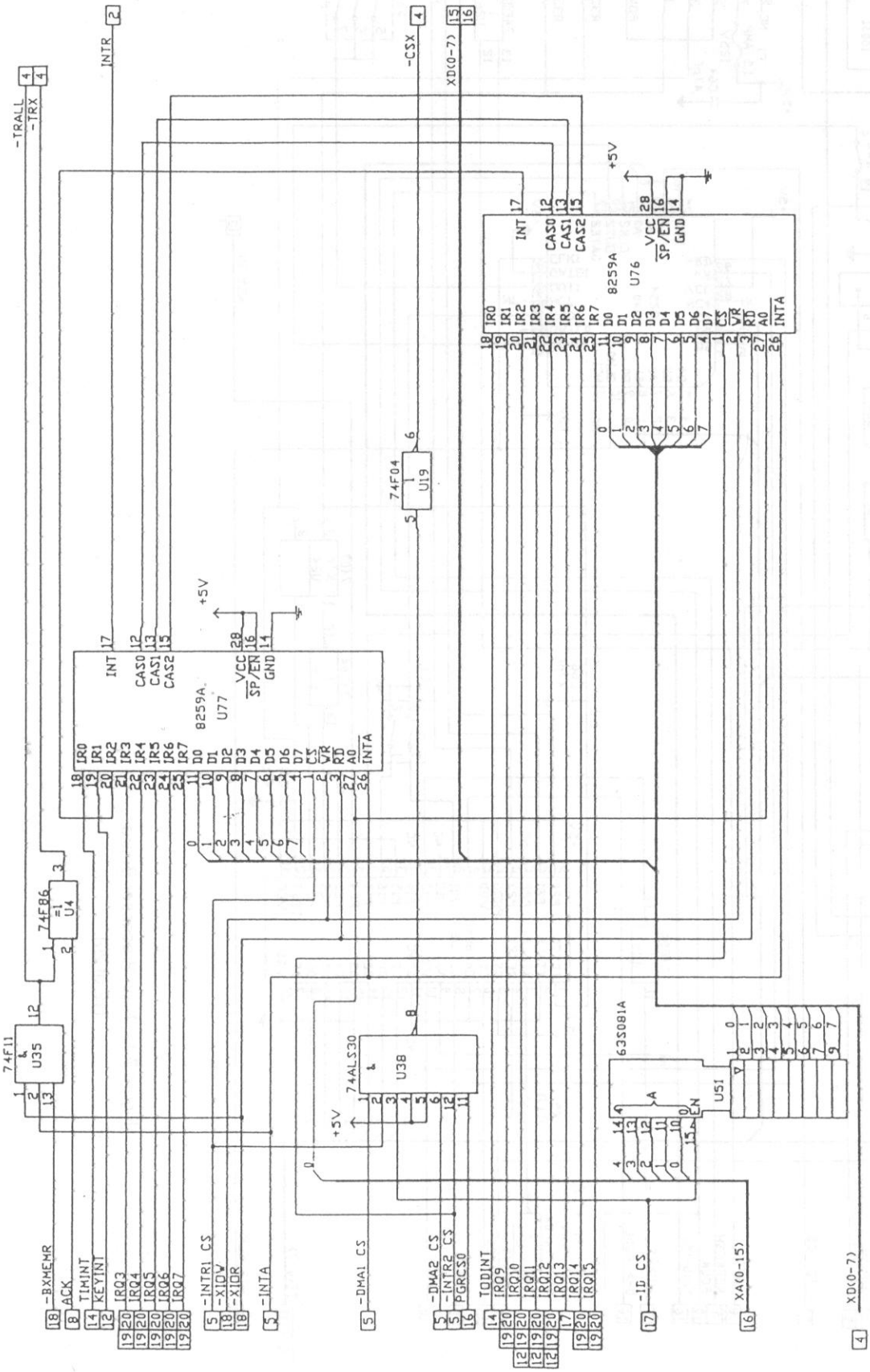

Figure 7-1 Main Processor Board
(13 of 20)

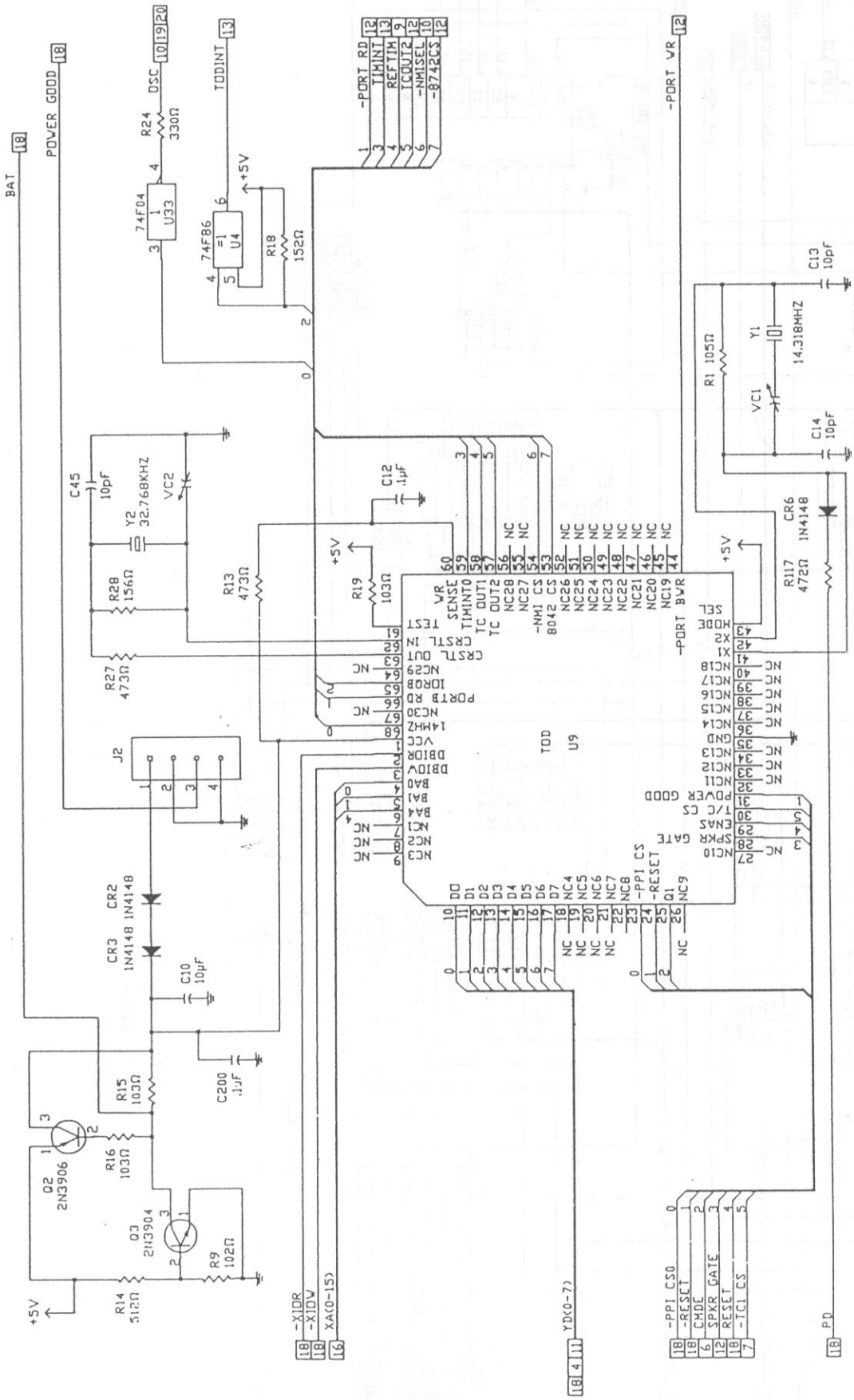

Figure 7-1 Main Processor Board
(14 of 20)

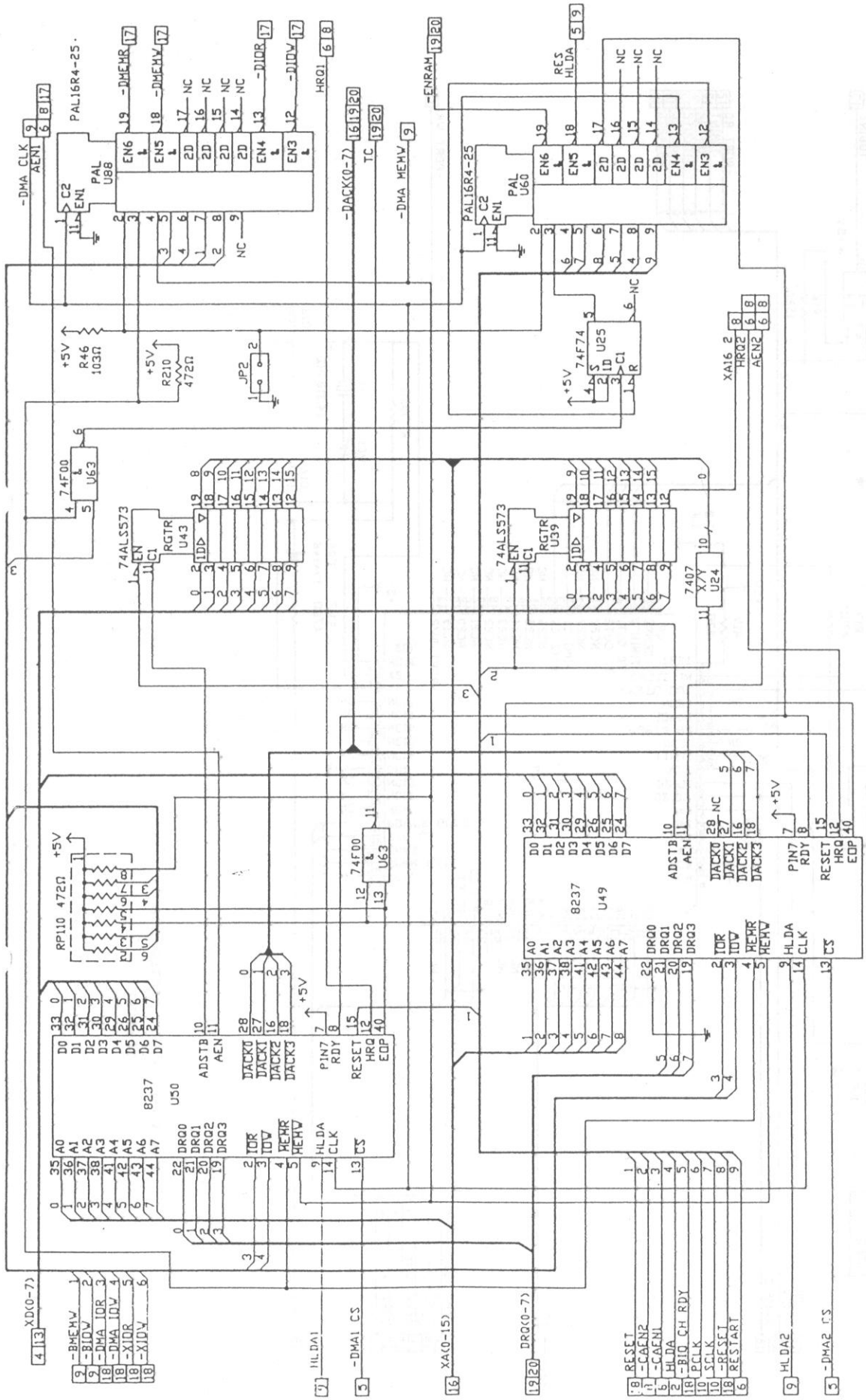

Figure 7-1 Main Processor Board
(15 of 20)

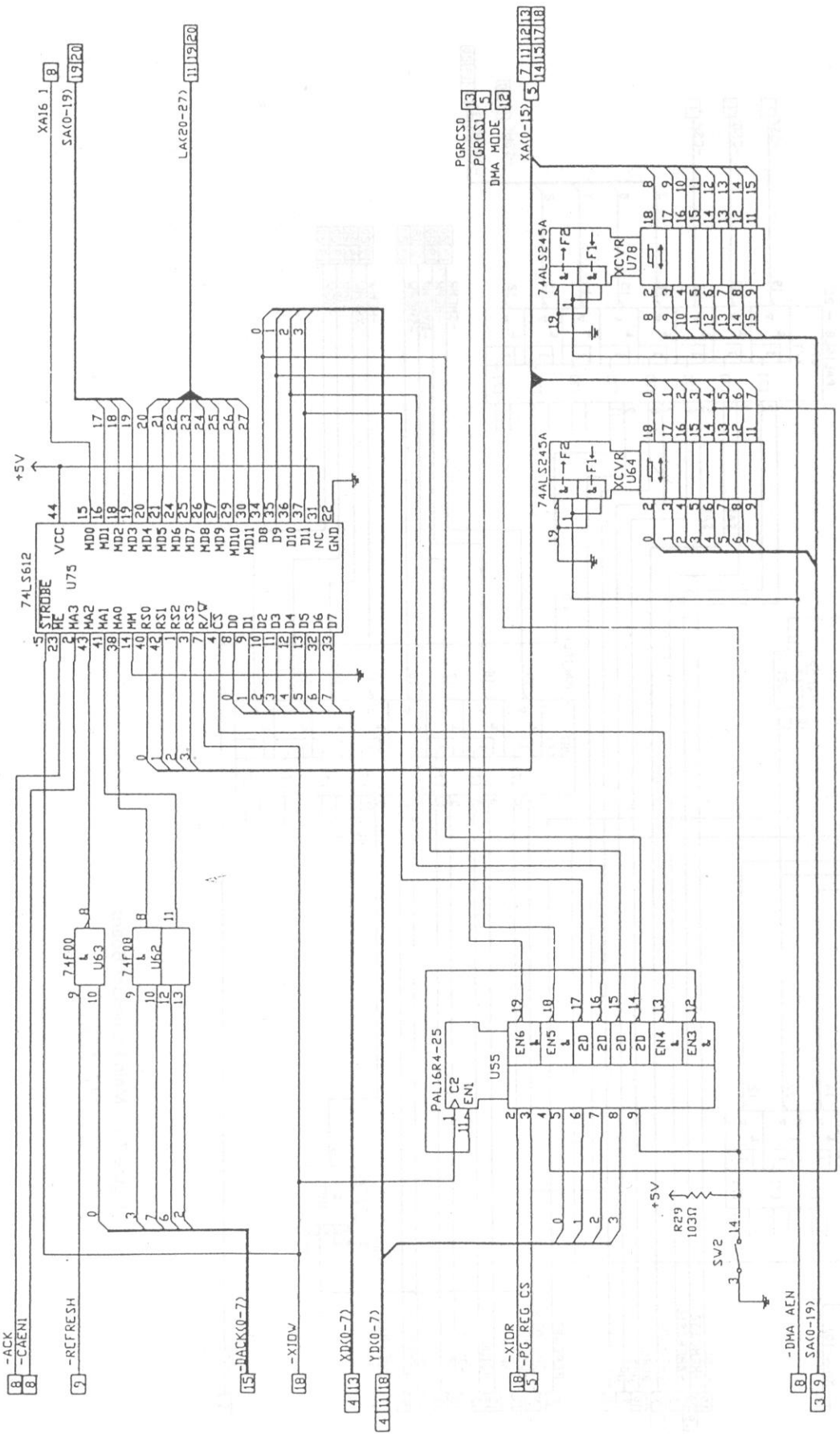

Figure 7-1 Main Processor Board
(16 of 20)

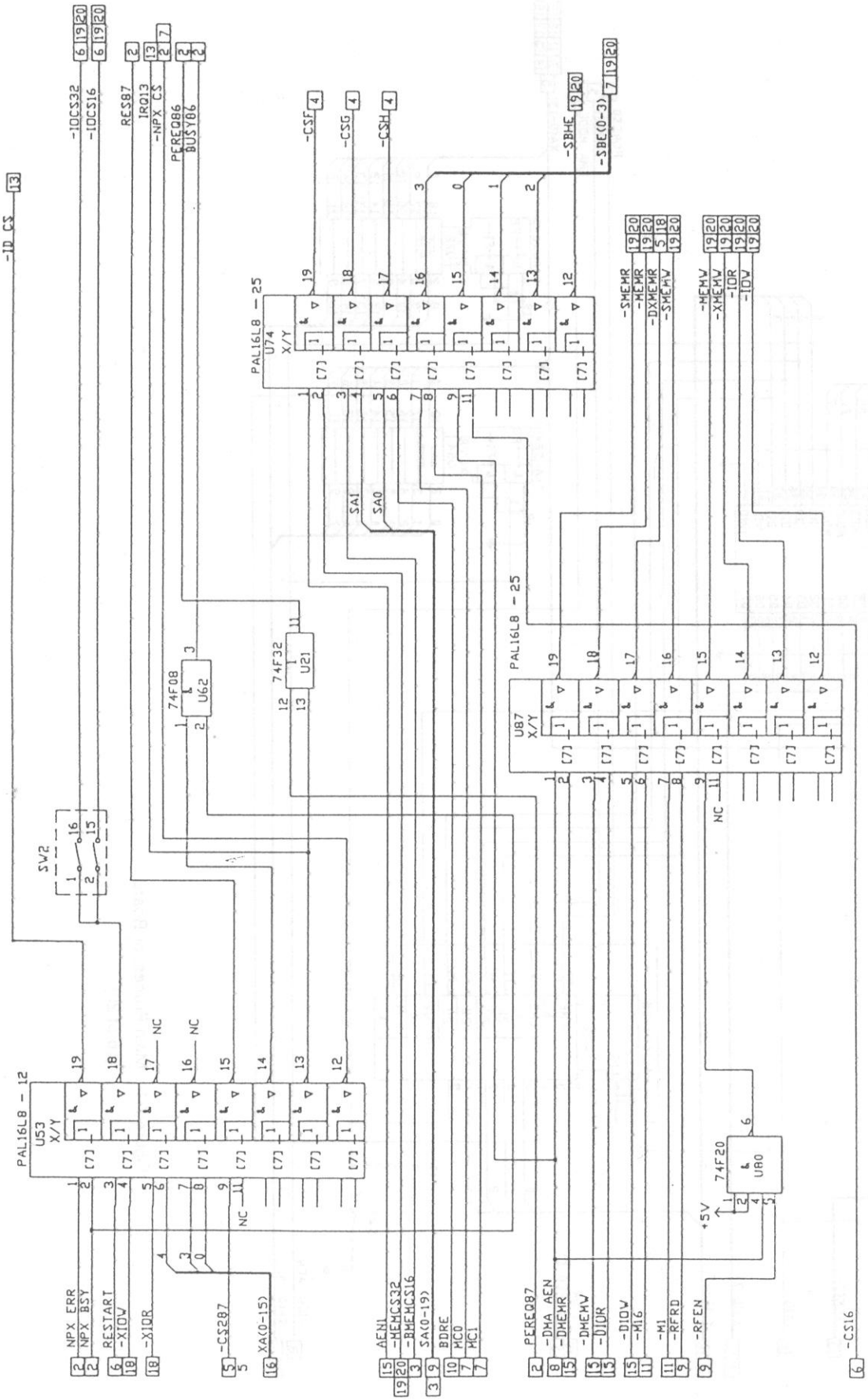

Figure 7-1 Main Processor Board
(17 of 20)

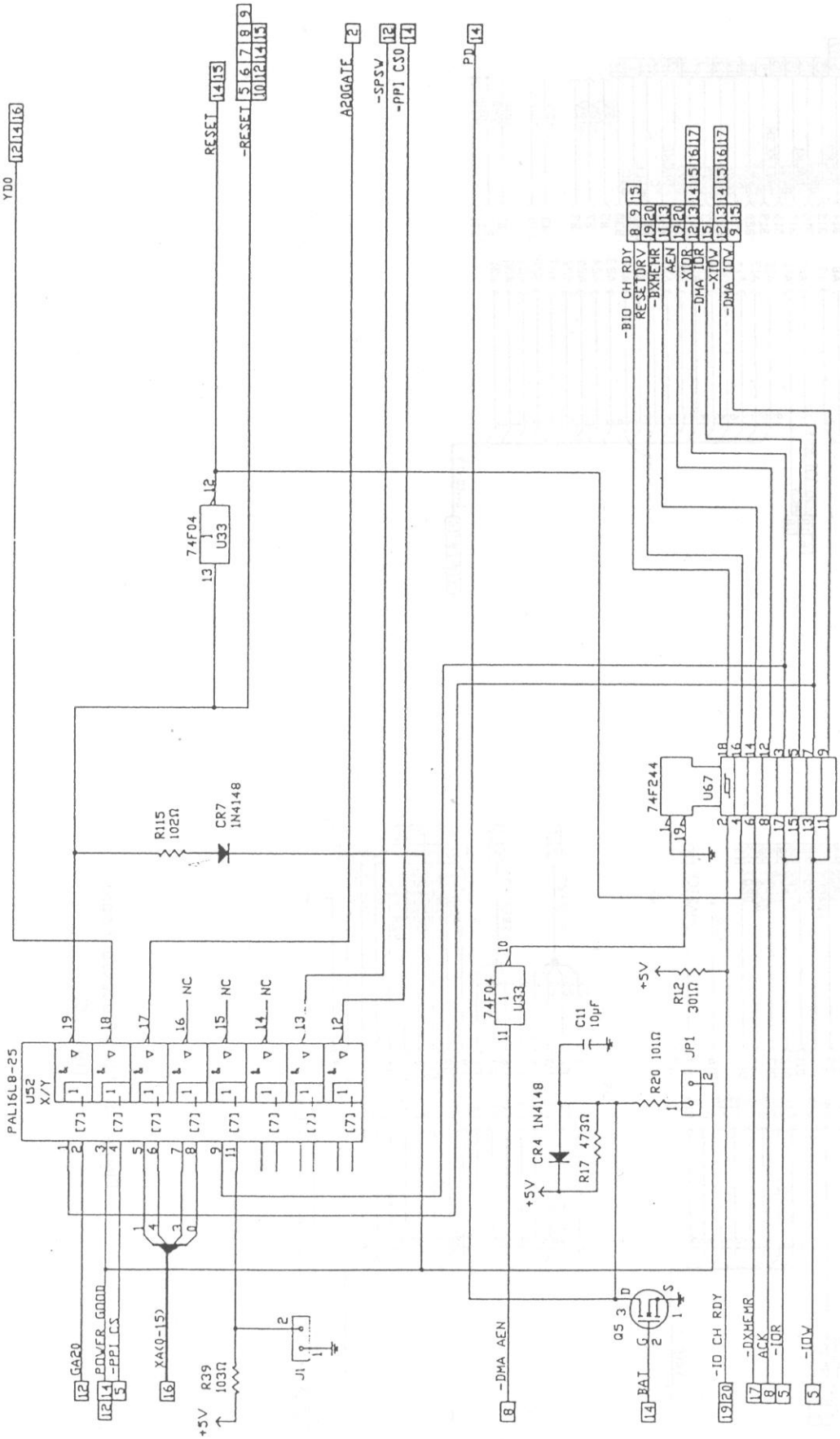

Figure 7-1 Main Processor Board
(18 of 20)

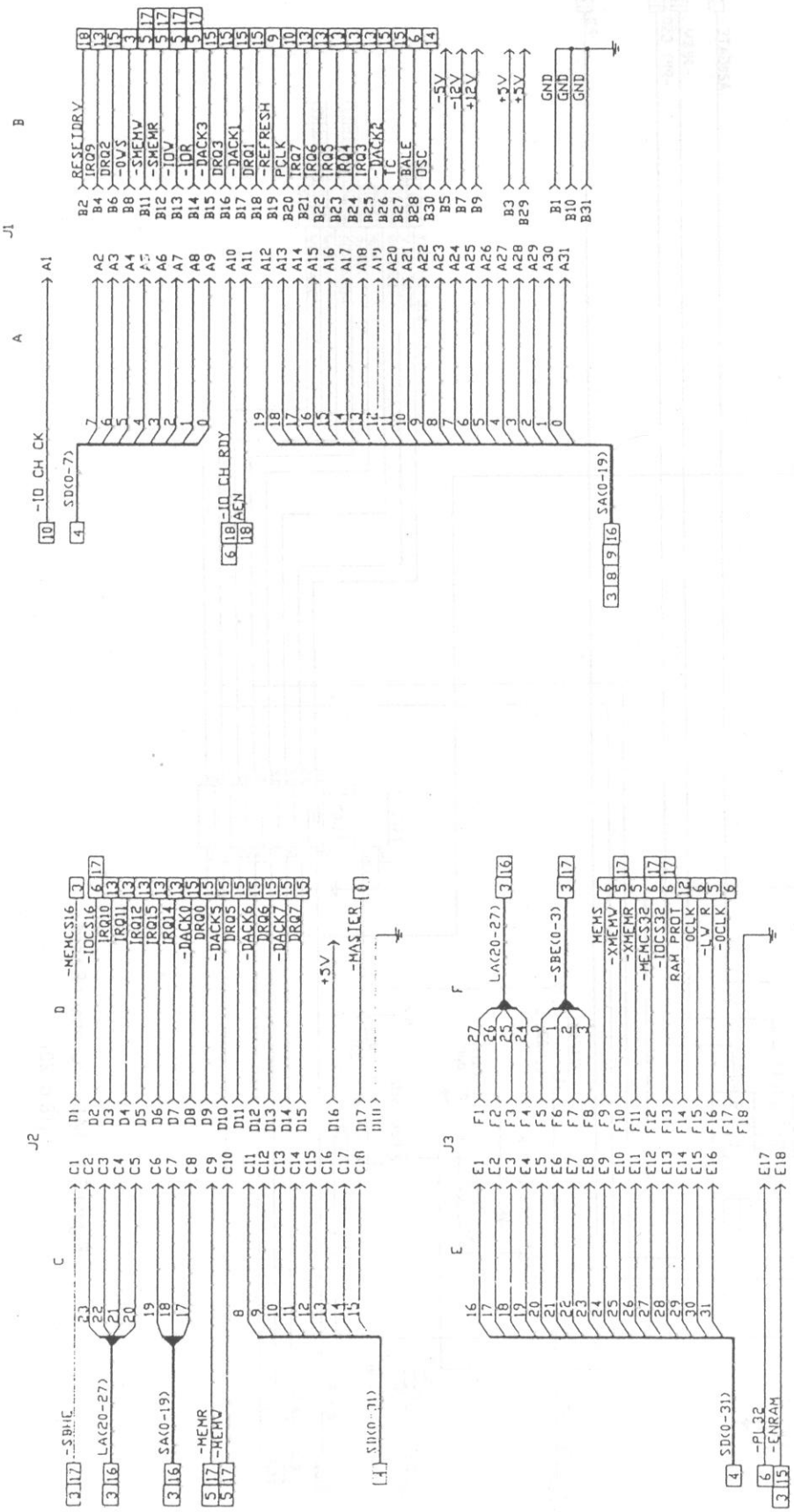

Figure 7-1 Main Processor Board
(19 of 20)

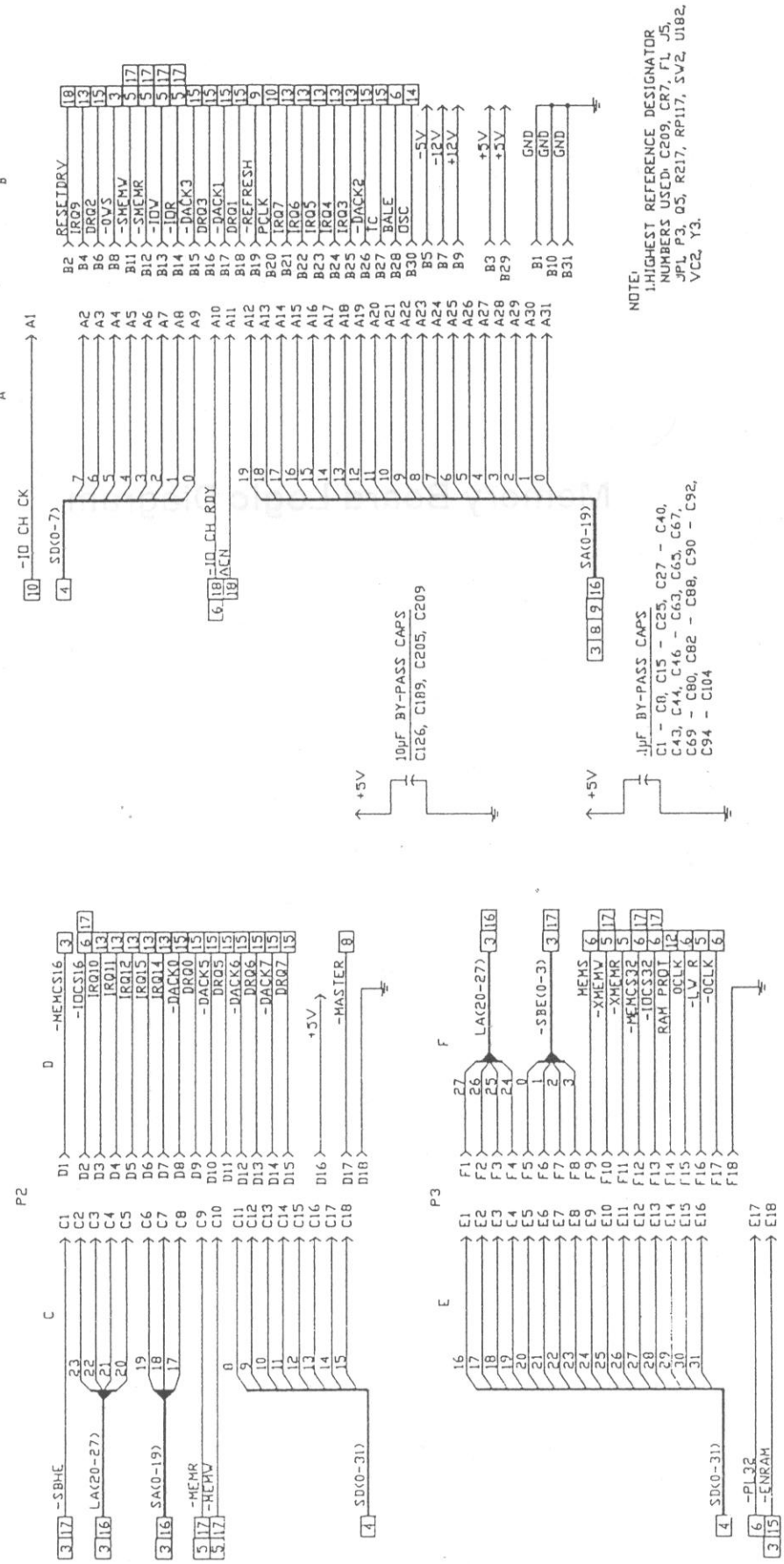

Figure 7-1 Main Processor Board
(20 of 20)

Memory Board Logic Diagram

U NUMBER	PIN NUMBERS +5	GND	UNUSED
1	8	16	
2	8	16	
3	8	16	
4	8	16	
5	20	10	
6	20	10	
7	20	10	
8	20	10	
9	8	16	
10	8	16	
11	8	16	
12	8	16	
13	8	16	
14	8	16	
15	8	16	
16	8	16	
17	8	16	
18	8	16	
19	8	16	
20	8	16	
21	8	16	
22	8	16	
23	8	16	
24	8	16	
25	1,16	8	
26	20	10	
27	20	10	
28			
29	5,9,13,14	7	
30			
31	8	16	
32	8	16	
33	8	16	
34	8	16	
35	8	16	
36	8	16	

U NUMBER	PIN NUMBERS +5	GND	UNUSED
37	8	16	
38	8	16	
39	8	16	
40	8	16	
41	8	16	
42	8	16	
43	8	16	
44	8	16	
45	8	16	
46	8	16	
47	16	8,15	
48	3,4,10,11,14	7	
49			
50	16	8,15	
51	8	16	
52	8	16	
53	8	16	
54	8	16	
55	8	16	
56	8	16	
57	8	16	
58	8	16	
59	8	16	
60	8	16	
61	8	16	
62	8	16	
63	8	16	
64	8	16	
65	8	16	
66	8	16	
67	16	8,10,11,13,14,15	
68	16	8,15	
69	1,10,13,14	7	
70			
71	16	8,15	
72	16	8,13,14,15	

U NUMBER	PIN NUMBERS +5	GND	UNUSED
73	8	16	
74	8	16	
75	8	16	
76	8	16	
77	8	16	
78	8	16	
79	8	16	
80	8	16	
81	8	16	
82	8	16	
83	8	16	
84	8	16	
85	8	16	
86	8	16	
87	8	16	
88	8	16	
89	7,11	18,19	
90	7,11	18,19	
91	20	10	
92	20	10	
93	7,11	18,19	
94	7,11	18,19	
95	8	16	
96	8	16	
97	8	16	
98	8	16	
99	20	2,3,10	
100	20	10	
101	14	4,5,7,13	
102	14	7	
103	2,16	8,14,15	
104	20	1,10	
105	20	1,10	
106			
107			
108			

U NUMBER	PIN NUMBERS +5	GND	UNUSED
109			
110			
111			
112			
113			
114			
115			
116			
117			
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119			
120			
121			
122			
123			
124			
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134			
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137			
138			
139			
140			
141			
142			
143			
144			

U NUMBER	PIN NUMBERS +5	GND	UNUSED
145			
146			
147			
148			
149			
150			
151			
152			
153			
154			
155			
156			
157			
158			
159			
160			
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179			
180			

Figure 7-2 Memory Board
(1 of 9)

LOGIC DIAGRAM

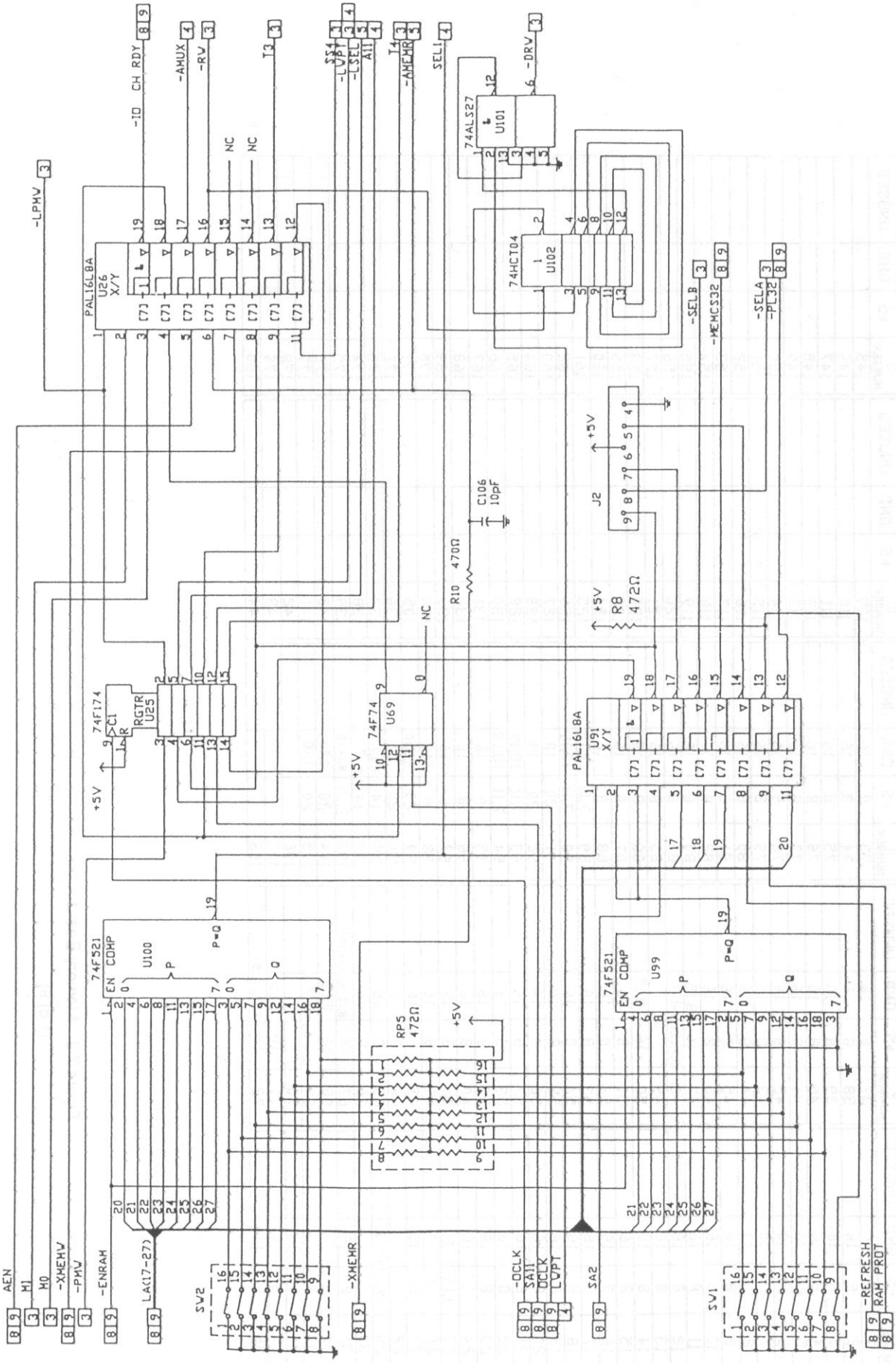

Figure 7-2 Memory Board
(2 of 9)

LOGIC DIAGRAM

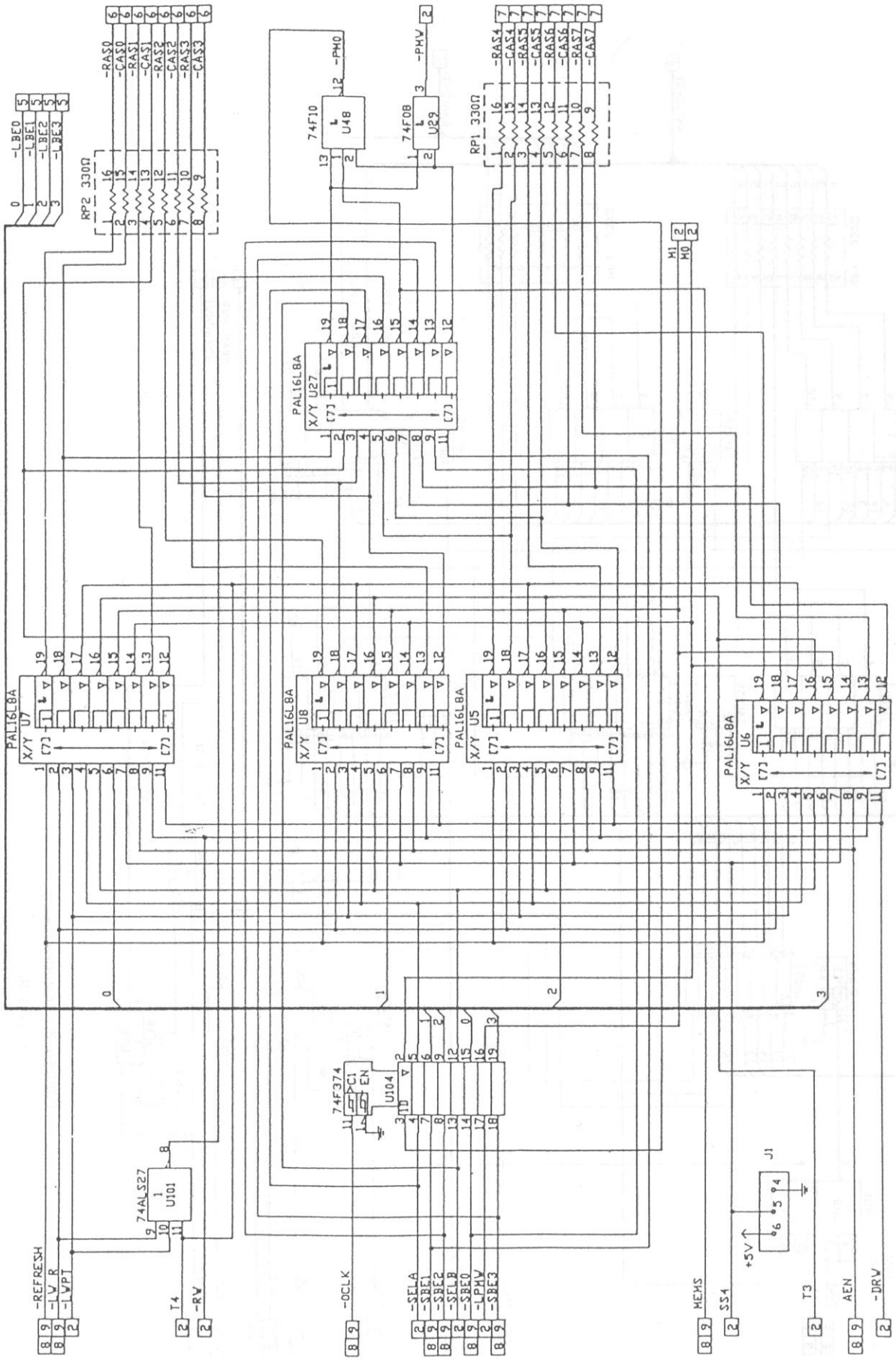

Figure 7-2 Memory Board
(3 of 9)

LOGIC DIAGRAM

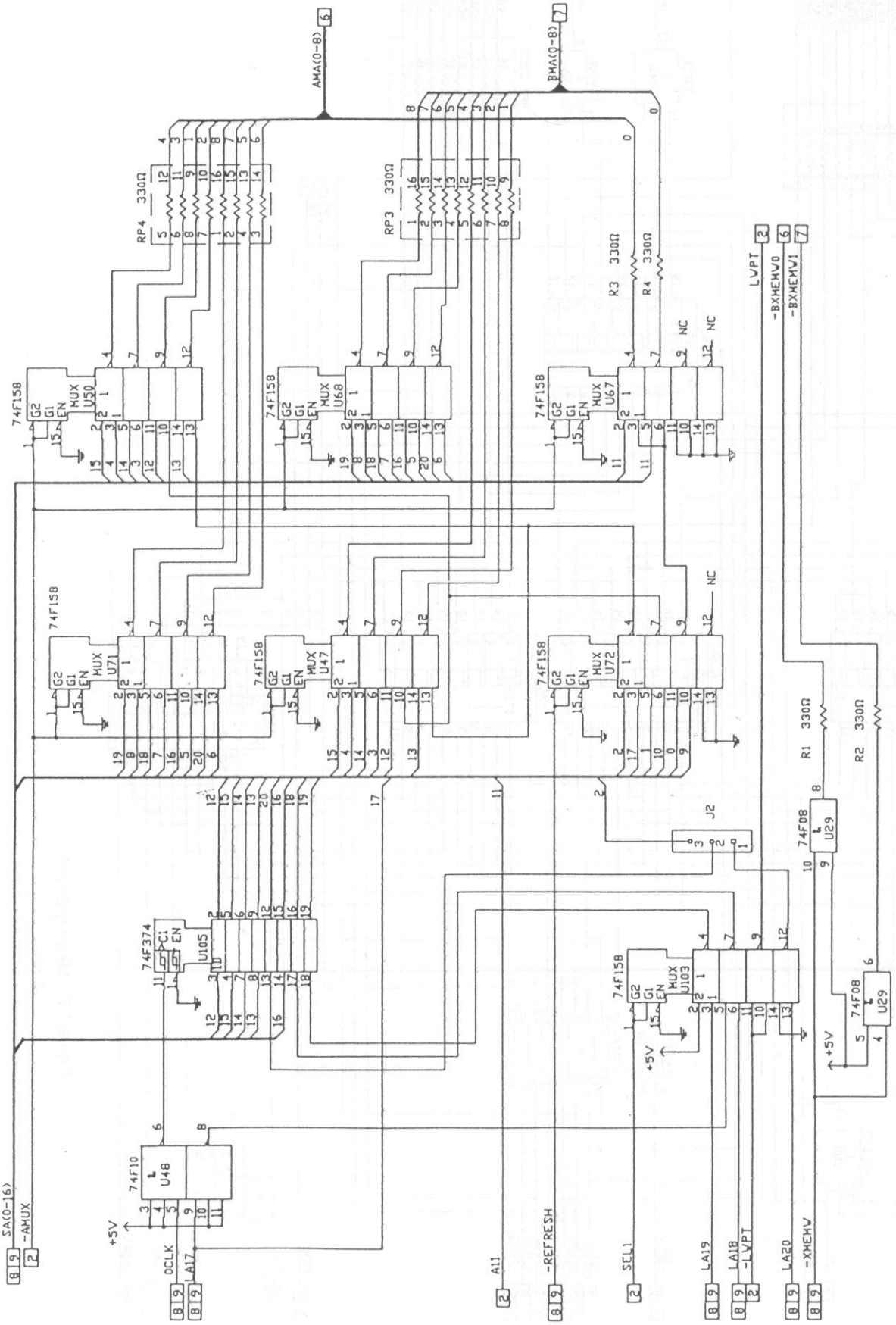

Figure 7-2 Memory Board
(4 of 9)

LOGIC DIAGRAM

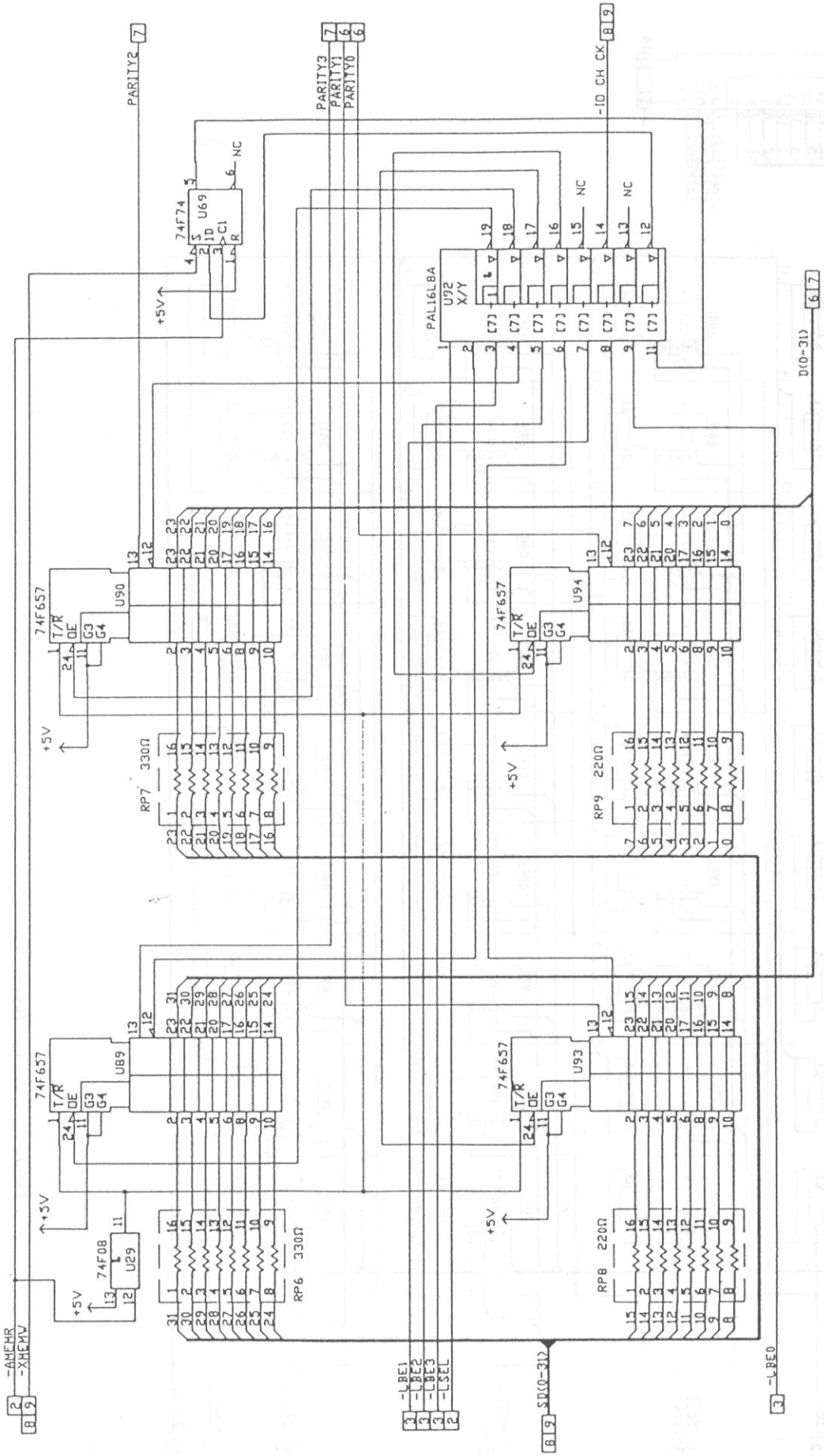

Figure 7-2 Memory Board
(5 of 9)

LOGIC DIAGRAM

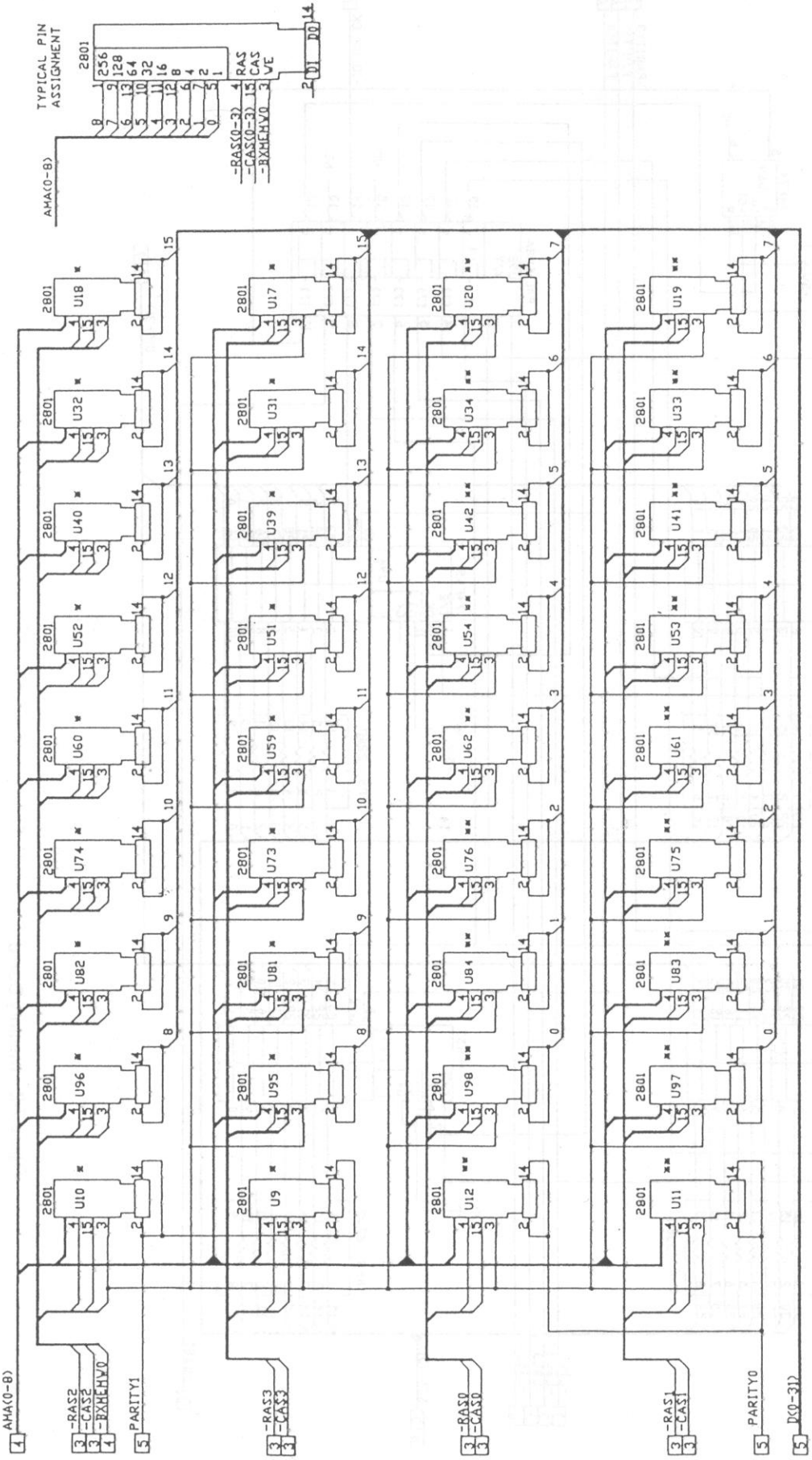

Figure 7-2 Memory Board
(6 of 9)

LOGIC DIAGRAM

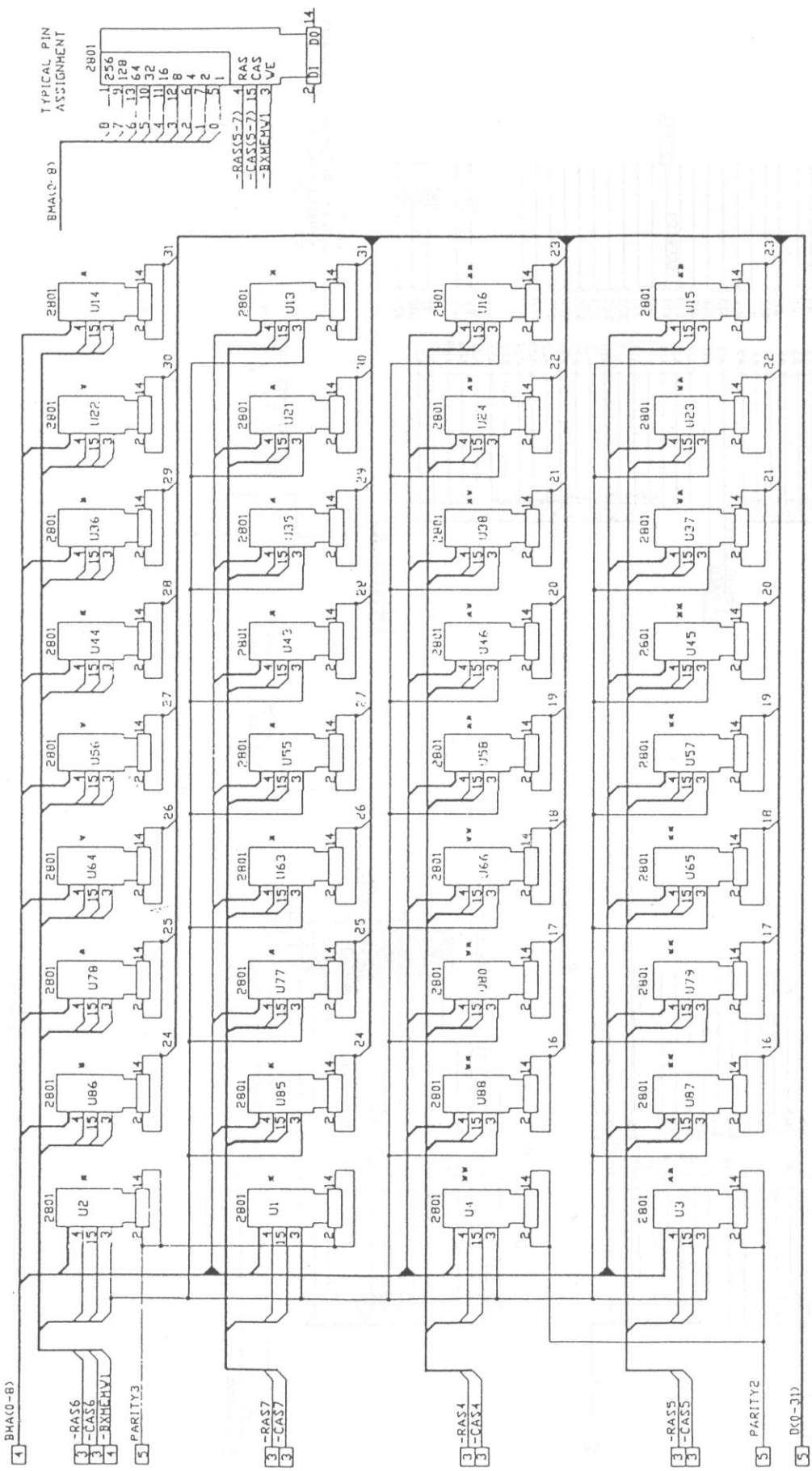

Figure 7-2 Memory Board
(7 of 9)

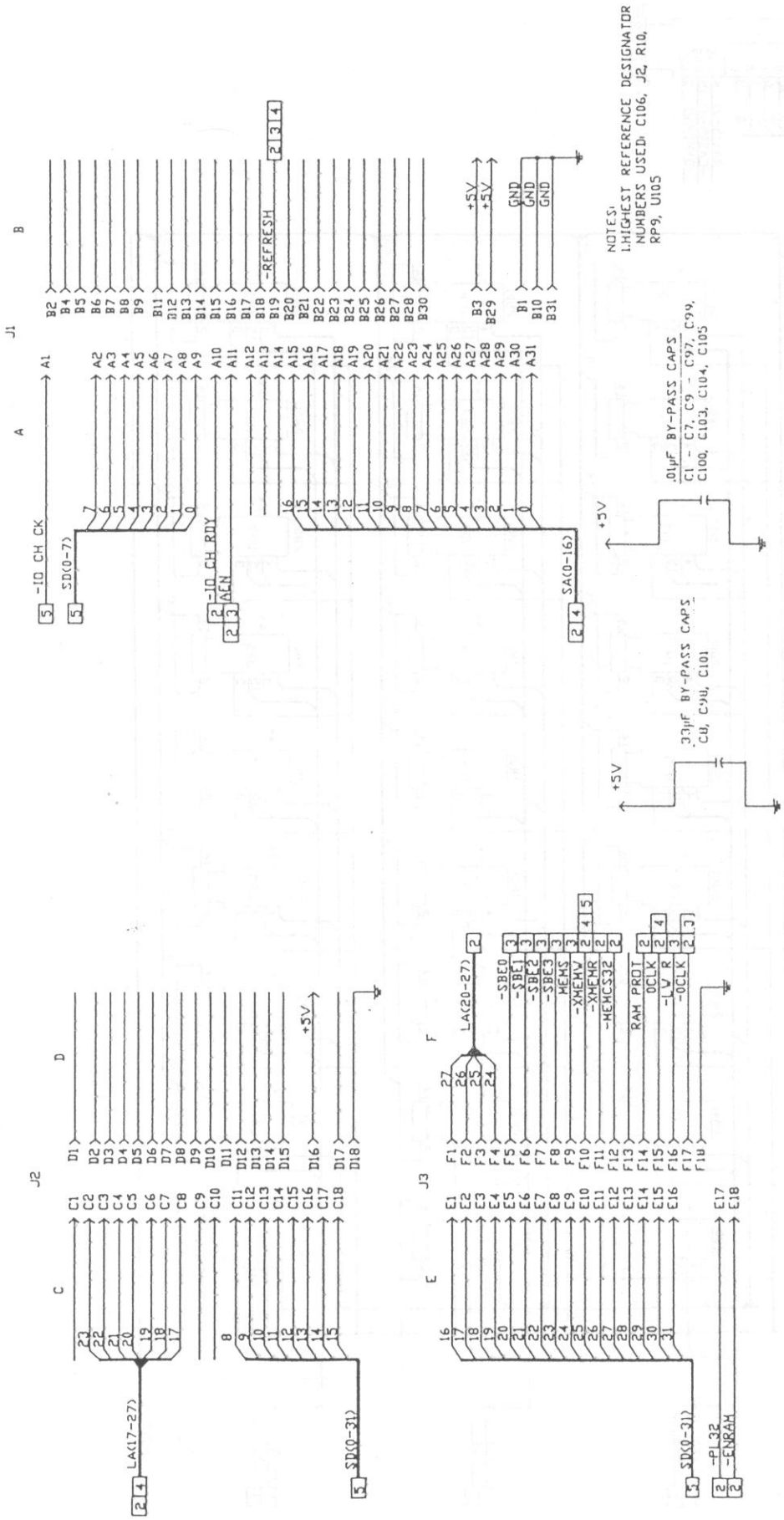

Figure 7-2 Memory Board
(8 of 9)

LOGIC DIAGRAM

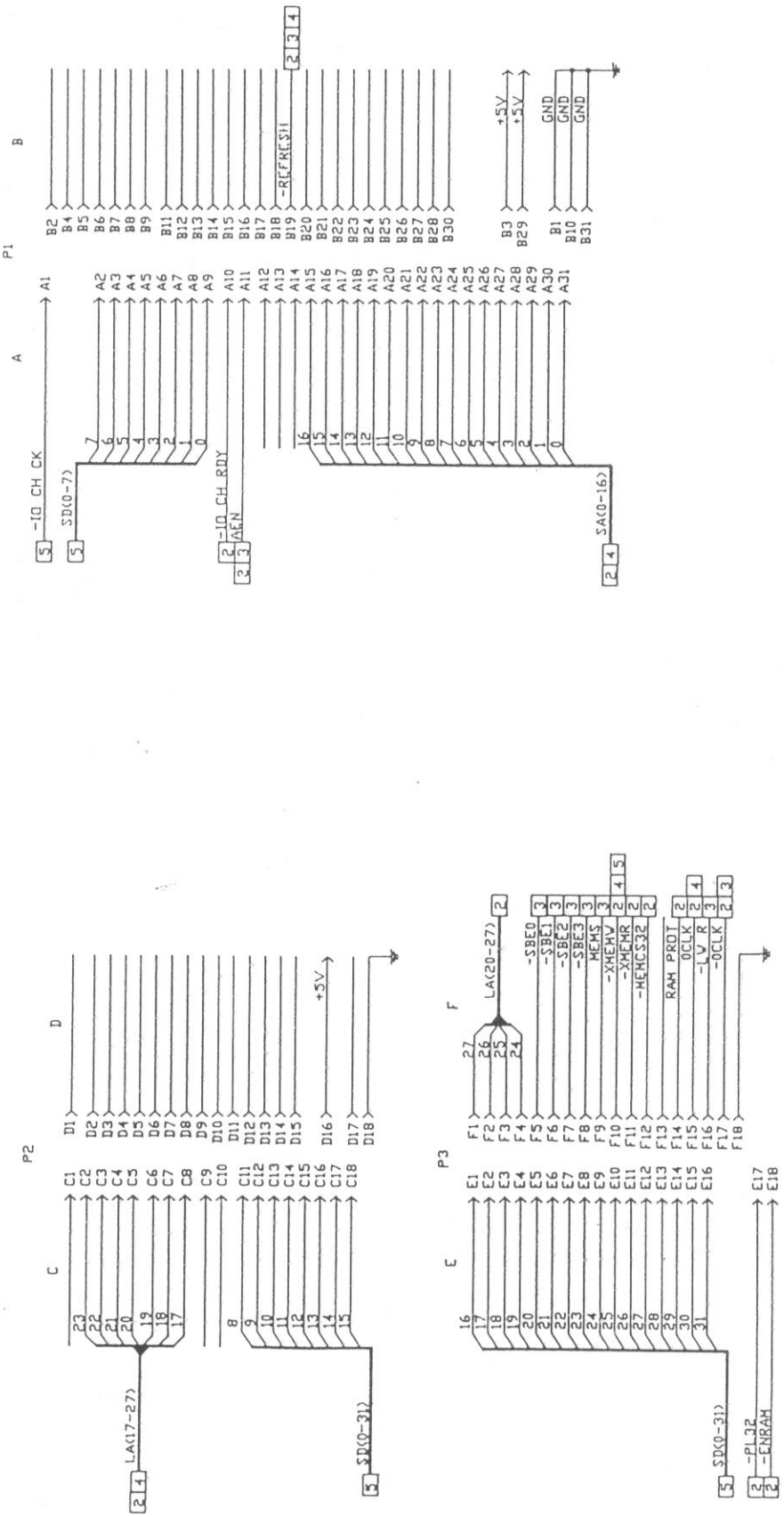

Figure 7-2 Memory Board
(9 of 9)

Chapter 8

80386 Instruction Set

The 80386 instruction set is presented on the following pages.

80386 Instruction Set Clock Count Summary

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
GENERAL DATA TRANSFER					
MOV = Move:					
Register to Register/Memory	1000100w mod reg r/m	2/2	2/2	b	h
Register/Memory to Register	1000101w mod reg r/m	2/4	2/4	b	h
Immediate to Register/Memory	1100011w mod 000 r/m immediate data	2/2	2/2	b	h
Immediate to Register (short form)	1011 w reg immediate data	2	2		
Memory to Accumulator (short form)	1010000w full displacement	4	4	b	h
Accumulator to Memory (short form)	1010001w full displacement	2	2	b	h
Register Memory to Segment Register	10001110 mod sreg3 r/m	2/5	18/19	b	h, i, j
Segment Register to Register/Memory	10001100 mod sreg3 r/m	2/2	2/2	b	h
MOVSX = Move With Sign Extension					
Register From Register/Memory	00001111 1011111w mod reg r/m	3/6	3/6	b	h
MOVZX = Move With Zero Extension					
Register From Register/Memory	00001111 1011011w mod reg r/m	3/6	3/6	b	h
PUSH = Push:					
Register/Memory	11111111 mod 110 r/m	5	5	b	h
Register (short form)	01010 reg	2	2	b	h
Segment Register (ES, CS, SS or DS) (short form)	000 sreg2 110	2	2	b	h
Segment Register (ES, CS, SS, DS, FS or GS)	00001111 10 sreg3 000	2	2	b	h
Immediate	011010s0 immediate data	2	2	b	h
PUSHA = Push All	01100000	18	18	b	h
POP = Pop					
Register/Memory	10001111 mod 000 r/m	5	5	b	h
Register (short form)	01011 reg	4	4	b	h
Segment Register (ES, CS, SS or DS) (short form)	000 sreg 2 111	7	21	b	h, i, j
Segment Register (ES, CS, SS or DS FS or GS)	00001111 10 sreg 3 001	7	21	b	h, i, j
POPA = Pop All	01100001	24	24	b	h
XCHG = Exchange					
Register/Memory With Register	1000011w mod reg r/m	3/5	3/5	b, f	f, h
Register With Accumulator (short form)	10010 reg	3	3		
IN = Input from:		Clk Count Virtual 8086 Mode			
Fixed Port	1110010w port number	†26	12	6*/26**	m
Variable Port	1110110w	†27	13	7*/27**	m
OUT = Output to:					
Fixed Port	1110011w port number	†24	10	4*/24**	m
Variable Port	1110111w	†25	11	5*/25**	m
LEA = Load EA to Register	10001101 mod reg r/m		2	2	

* If CPL ≤ IOPL ** If CPL > IOPL

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
SEGMENT CONTROL					
LDS = Load Pointer to DS	11000101 | mod reg r/m	7	22	b	h, i, j
LES = Load Pointer to ES	11000100 | mod reg r/m	7	22	b	h, i, j
LFS = Load Pointer to FS	00001111 | 10110100 | mod reg r/m	7	25	b	h, i, j
LGS = Load Pointer to GS	00001111 | 10110101 | mod reg r/m	7	25	b	h, i, j
LSS = Load Pointer to SS	00001111 | 10110010 | mod reg r/m	7	22	b	h, i, j
FLAG CONTROL					
CLC = Clear Carry Flag	11111000	2	2		
CLD = Clear Direction Flag	11111100	2	2		
CLI = Clear Interrupt Enable Flag	11111010	3	3		m
CLTS = Clear Task Switched Flag	00001111 | 00000110	5	5	c	l
CMC = Complement Carry Flag	11110101	2	2		
LAHF = Load AH into Flag	10011111	2	2		
POPF = Pop Flags	10011101	5	5	b	h, n
PUSHF = Push Flags	10011100	4	4	b	h
SAHF = Store AH into Flags	10011110	3	3		
STC = Set Carry Flag	11111001	2	2		
STD = Set Direction Flag	11111001	2	2		
STI = Set Interrupt Enable Flag	11111011	3	3		m
ARITHMETIC					
ADD = Add					
Register to Register	000000dw | mod reg r/m	2	2		
Register to Memory	0000000w | mod reg r/m	7	7	b	h
Memory to Register	0000001w | mod reg r/m	6	6	b	h
Immediate to Register/Memory	100000sw | mod 000 r/m | immediate data	2/7	2/7	b	h
Immediate to Accumulator (short form)	0000010w | immediate data	2	2		
ADC = Add With Carry					
Register to Register	000100dw | mod reg r/m	2	2		
Register to Memory	0001000w | mod reg r/m	7	7	b	h
Memory to Register	0001001w | mod reg r/m	6	6	b	h
Immediate to Register/Memory	100000sw | mod 010 r/m | immediate data	2/7	2/7	b	h
Immediate to Accumulator (short form)	0001010w | immediate data	2	2		
INC = Increment					
Register/Memory	1111111w | mod 000 r/m	2/6	2/6	b	h
Register (short form)	01000 reg	2	2		
SUB = Subtract					
Register from Register	001010dw | mod reg r/m	2	2		

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT		NOTES	
		Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode
ARITHMETIC (Continued)					
Register from Memory	0010100w mod reg r/m	7	7	b	h
Memory from Register	0010101w mod reg r/m	6	6	b	h
Immediate from Register/Memory	100000sw mod101 r/m immediate data	2/7	2/7	b	h
Immediate from Accumulator (short form)	0010110w immediate data	2	2		
SBB = Subtract with Borrow					
Register from Register	000110dw mod reg r/m	2	2		
Register from Memory	0001100w mod reg r/m	7	7	b	h
Memory from Register	0001101w mod reg r/m	6	6	b	h
Immediate from Register/Memory	100000sw mod011 r/m immediate data	2/7	2/7	b	h
Immediate from Accumulator (short form)	0001110w immediate data	2	2		
DEC = Decrement					
Register/Memory	1111111w reg001 r/m	2/6	2/6	b	h
Register (short form)	01001 reg	2	2		
CMP = Compare					
Register with Register	001110dw mod reg r/m	2	2		
Memory with Register	0011100w mod reg r/m	5	5	b	h
Register with Memory	0011101w mod reg r/m	6	6	b	h
Immediate with Register/Memory	100000sw mod111 r/m immediate data	2/5	2/5	b	h
Immediate with Accumulator (short form)	0011110w immediate data	2	2		
NEG = Change Sign	1111011w mod011 r/m	2/6	2/6	b	h
AAA = ASCII Adjust for Add	00110111	4	4		
AAS = ASCII Adjust for Subtract	00111111	4	4		
DAA = Decimal Adjust for Add	00100111	4	4		
DAS = Decimal Adjust for Subtract	00101111	4	4		
MUL = Multiply (unsigned)					
Accumulator with Register/Memory	1111011w mod100 r/m				
Multiplier-Byte		9-14/12-17	9-14/12-17	b, d	d, h
-Word		9-22/12-25	9-22/12-25	b, d	d, h
-Doubleword		9-38/12-41	9-38/12-41	b, d	d, h
IMUL = Integer Multiply (signed)					
Accumulator with Register/Memory	1111011w mod100 r/m				
Multiplier-Byte		9-14/12-17	9-14/12-17	b, d	d, h
-Word		9-22/12-25	9-22/12-25	b, d	d, h
-Doubleword		9-38/12-41	9-38/12-41	b, d	d, h
Register with Register/Memory	00001111 10101111 mod reg r/m				
-Word		9-22/12-25	9-22/12-25	b, d	d, h
-Doubleword		9-38/12-41	9-38/12-41	b, d	d, h
Register/Memory with Immediate to Register	011010s1 mod reg r/m immediate data				
-Word		9-22/12-25	9-22/12-25	b, d	d, h
-Doubleword		9-38/12-41	9-38/12-41	b, d	d, h

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
ARITHMETIC (Continued)					
DIV = Divide (Unsigned)					
Accumulator by Register/Memory	1111011 w | mod 110 r/m				
Divisor—Byte		14/17	14/17	b,e	e,h
—Word		22/25	22/25	b,e	e,h
—Doubleword		38/41	38/41	b,e	e,h
IDIV = Integer Divide (Signed)					
Accumulator By Register/Memory	1111011 w | mod 111 r/m				
Divisor—Byte		19/22	19/22	b,e	e,h
—Word		27/30	27/30	b,e	e,h
—Doubleword		43/46	43/46	b,e	e,h
AAD = ASCII Adjust for Divide	11010101 | 00001010	19	19		
AAM = ASCII Adjust for Multiply	11010100 | 00001010	17	17		
CBW = Convert Byte to Word	10011000	3	3		
CWD = Convert Word to Double Word	10011001	2	2		
LOGIC					
Shift Rotate Instructions					
Not Through Carry (ROL, ROR, SAL, SAR, SHL, and SHR)					
Register/Memory by 1	1101000 w | mod TTT r/m	3/7	3/7	b	h
Register/Memory by CL	1101001 w | mod TTT r/m	3/7	3/7	b	h
Register/Memory by Immediate Count	1100000 w | mod TTT r/m | immed 8-bit data	3/7	3/7	b	h
Through Carry (RCL and RCR)					
Register/Memory by 1	1101000 w | mod TTT r/m	9/10	9/10	b	h
Register/Memory by CL	1101001 w | mod TTT r/m	9/10	9/10	b	h
Register/Memory by Immediate Count	1100000 w | mod TTT r/m | immed 8-bit data	9/10	9/10	b	h
SHLD = Shift Left Double					
Register/Memory by Immediate	00001111 | 10100100 | mod reg r/m | immed 8-bit data	3/7	3/7		
Register/Memory by CL	00001111 | 10100101 | mod reg r/m	3/7	3/7		
SHRD = Shift Right Double					
Register/Memory by Immediate	00001111 | 10101100 | mod reg r/m | immed 8-bit data	3/7	3/7		
Register/Memory by CL	00001111 | 10101101 | mod reg r/m	3/7	3/7		
AND = And					
Register to Register	001000 d w | mod reg r/m	2	2		

TTT	Instruction
000	ROL
001	ROR
010	RCL
011	RCR
100	SHL/SAL
101	SHR
111	SAR

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	Clk Count Virtual 8086 Mode	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
LOGIC (Continued)						
Register to Memory	0010000w mod reg r/m		7	7	b	h
Memory to Register	0010001w mod reg r/m		6	6	b	h
Immediate to Register/Memory	1000000w mod 100 r/m immediate data		2/7	2/7	b	h
Immediate to Accumulator (Short Form)	0010010w immediate data		2	2		
TEST = And Function to Flags, No Result						
Register/Memory and Register	1000010w mod reg r/m		2/5	2/5	b	h
Immediate Data and Register/Memory	1111011w mod 000 r/m immediate data		2/5	2/5	b	h
Immediate Data and Accumulator (Short Form)	1010100w immediate data		2	2		
OR = Or						
Register to Register	000010dw mod reg r/m		2	2		
Register to Memory	0000100w mod reg r/m		7	7	b	h
Memory to Register	0000101w mod reg r/m		6	6	b	h
Immediate to Register/Memory	1000000w mod 001 r/m immediate data		2/7	2/7	b	h
Immediate to Accumulator (Short Form)	0000110w immediate data		2	2		
XOR = Exclusive Or						
Register to Register	001100dw mod reg r/m		2	2		
Register to Memory	0011000w mod reg r/m		7	7	b	h
Memory to Register	0011001w mod reg r/m		6	6	b	h
Immediate to Register/Memory	1000000w mod 110 r/m immediate data		2/7	2/7	b	h
Immediate to Accumulator (Short Form)	0011010w immediate data		2	2		
NOT = Invert Register/Memory	1111011w mod 010 r/m		2/6	2/6	b	h
STRING MANIPULATION						
CMPS = Compare Byte Word	1010011w		10	10	b	h
INS = Input Byte/Word from DX Port	0110110w	†29	15	9*/29**	b	h, m
LODS = Load Byte/Word to AL/AX/EAX	1010110w		5	5	b	h
MOVS = Move Byte Word	1010010w		7	7	b	h
OUTS = Output Byte/Word to DX Port	0110111w	†28	14	8*/28**	b	h, m
SCAS = Scan Byte Word	1010111w		7	7	b	h
STOS = Store Byte/Word from AL/AX/EX	1010101w		4	4	b	h
XLAT = Translate String	11010111		5	5		h
REPEATED STRING MANIPULATION						
Repeated by Count in CX or ECX						
REPE CMPS = Compare String (Find Non-Match)	11110011 1010011w		5+9n	5+9n	b	h

* If CPL ≤ IOPL ** If CPL > IOPL

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
REPEATED STRING MANIPULATION (Continued)					
REPNE CMPS = Compare String (Find Match)	11110010 1010011w — Clk Count Virtual 8086 Mode	5 + 9n	5 + 9n	b	h
REP INS = Input String	11110010 0110110w	†27 + 6n			
REP LODS = Load String	11110010 1010110w	13 + 6n	7 + 6n°/27 + 6n°°	b	h, m
REP MOVS = Move String	11110010 1010010w	5 + 6n	5 + 6n	b	h
REP OUTS = Output String	11110010 0110111w — †26 + 5n	7 + 4n	7 + 4n	b	h
REPE SCAS = Scan String (Find Non-AL/AX/EAX)	11110011 1010111w	12 + 5n	6 + 5n°/26 + 5n°°	b	h, m
REPNE SCAS = Scan String (Find AL/AX/EAX)	11110010 1010111w	5 + 8n	5 + 8n	b	h
REP STOS = Store String	11110010 1010101w	5 + 8n	5 + 8n	b	h
		5 + 5n	5 + 5n	b	h
BIT MANIPULATION					
BSF = Scan Bit Forward	00001111 10111100 mod reg r/m	10 + 3n	10 + 3n	b	h
BSR = Scan Bit Reverse	00001111 10111101 mod reg r/m	10 + 3n	10 + 3n	b	h
BT = Test Bit					
Register/Memory, Immediate	00001111 10111010 mod 100 r/m immed 8-bit data	3/6	3/6	b	h
Register/Memory, Register	00001111 10100011 mod reg r/m	3/12	3/12	b	h
BTC = Test Bit and Complement					
Register/Memory, Immediate	00001111 10111010 mod 111 r/m immed 8-bit data	6/8	6/8	b	h
Register/Memory, Register	00001111 10111011 mod reg r/m	6/13	6/13	b	h
BTR = Test Bit and Reset					
Register/Memory, Immediate	00001111 10111010 mod 110 r/m immed 8-bit data	6/8	6/8	b	
Register/Memory, Register	00001111 10110011 mod reg r/m	6/13	6/13	b	
BTS = Test Bit and Set					
Register/Memory, Immediate	00001111 10111010 mod 101 r/m immed 8-bit data	6/8	6/8	b	h
Register/Memory, Register	00001111 10101011 mod reg r/m	6/13	6/13	b	h
CONTROL TRANSFER					
CALL = Call					
Direct Within Segment	11101000 full displacement	7 + m	7 + m	b	r
Register/Memory					
Indirect Within Segment	11111111 mod 010 r/m	7 + m/ 10 + m	7 + m/ 10 + m	b	h, r
Direct Intersegment	10011010 unsigned full offset, selector	17 + m	34 + m	b	j,k,r

Notes:
† Clock count shown applies if I/O permission allows I/O to the port in virtual 8086 mode. If I/O bit map denies permission exception 13 fault occurs; refer to clock counts for INT 3 instruction.
° If CPL ≤ IOPL °° If CPL > IOPL

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT		NOTES	
		Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode
CONTROL TRANSFER (Continued)					
Protected Mode Only (Direct Intersegment)					
Via Call Gate to Same Privilege Level			52 + m		h,i,k,r
Via Call Gate to Different Privilege Level, (No Parameters)			86 + m		h,i,k,r
Via Call Gate to Different Privilege Level, (x Parameters)			94 + 4x + m		h,i,k,r
From 286 Task to 286 TSS			273		h,i,k,r
From 286 Task to 386 TSS			298		h,i,k,r
From 286 Task to Virtual 8086 Task (386 TSS)			217		h,i,k,r
From 386 Task to 286 TSS			273		h,i,k,r
From 386 Task to 386 TSS			300		h,i,k,r
From 386 Task to Virtual 8086 Task (386 TSS)			217		h,i,k,r
Indirect Intersegment	11111111 mod 011 r/m	22 + m	38 + m	b	h,i,k,r
Protected Mode Only (Indirect Intersegment)					
Via Call Gate to Same Privilege Level			56 + m		h,i,k,r
Via Call Gate to Different Privilege Level, (No Parameters)			90 + m		h,i,k,r
Via Call Gate to Different Privilege Level, (x Parameters)			98 + 4x + m		h,i,k,r
From 286 Task to 286 TSS			278		h,i,k,r
From 286 Task to 386 TSS			303		h,i,k,r
From 286 Task to Virtual 8086 Task (386 TSS)			221		h,i,k,r
From 386 Task to 286 TSS			278		h,i,k,r
From 386 Task to 386 TSS			305		h,i,k,r
From 386 Task to Virtual 8086 Task (386 TSS)			221		h,i,k,r
JMP = Unconditional Jump					
Short	11101001 8-bit displacement	7 + m	7 + m		r
Direct within Segment	11101001 full displacement	7 + m	7 + m		r
Register/Memory Indirect within Segment	11111111 mod 100 r/m	7 + m/ 10 + m	7 + m/ 10 + m	b	h,r
Direct Intersegment	11101010 unsigned full offset, selector	12 + m	27 + m		j,k,r
Protected Mode Only (Direct Intersegment)					
Via Call Gate to Same Privilege Level			45 + m		h,i,k,r
From 286 Task to 286 TSS			274		h,i,k,r
From 286 Task to 386 TSS			301		h,i,k,r
From 286 Task to Virtual 8086 Task (386 TSS)			218		h,i,k,r
From 386 Task to 286 TSS			270		h,i,k,r
From 386 Task to 386 TSS			303		h,i,k,r
From 386 Task to Virtual 8086 Task (386 TSS)			220		h,i,k,r
Indirect Intersegment	11111111 mod 101 r/m	17 + m	31 + m	b	h,i,k,r
Protected Mode Only (Indirect Intersegment)					
Via Call Gate to Same Privilege Level			49 + m		h,i,k,r
From 286 Task to 286 TSS			279		h,i,k,r
From 286 Task to 386 TSS			306		h,i,k,r
From 286 Task to Virtual 8086 Task (386 TSS)			222		h,i,k,r
From 386 Task to 286 TSS			275		h,i,k,r
From 386 Task to 386 TSS			308		h,i,k,r
From 386 Task to Virtual 8086 Task (386 TSS)			224		h,i,k,r

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
CONTROL TRANSFER (Continued)					
RET = Return from CALL:					
Within Segment	11000011	10 + m	10 + m	b	g, h, r
Within Segment Adding Immediate to SP	11000010 | 16-bit displ	10 + m	10 + m	b	g, h, r
Intersegment	11001011	18 + m	32 + m	b	g, h, j, k, r
Intersegment Adding Immediate to SP	11001010 | 16-bit displ	18 + m	32 + m	b	g, h, j, k, r
Protected Mode Only (RET):					
to Different Privilege Level			68		h, j, k, r
Intersegment			68		h, j, k, r
Intersegment Adding Immediate to SP					
CONDITIONAL JUMPS					
NOTE: Times Are Jump "Taken or Not Taken"					
JO = Jump on Overflow					
8-Bit Displacement	01110000 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000000 | full displacement	7 + m or 3	7 + m or 3		r
JNO = Jump on Not Overflow					
8-Bit Displacement	01110001 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000001 | full displacement	7 + m or 3	7 + m or 3		r
JB/JNAE = Jump on Below/Not Above or Equal					
8-Bit Displacement	01110010 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000010 | full displacement	7 + m or 3	7 + m or 3		r
JNB/JAE = Jump on Not Below/Above or Equal					
8-Bit Displacement	01110011 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000011 | full displacement	7 + m or 3	7 + m or 3		r
JE/JZ = Jump on Equal/Zero					
8-Bit Displacement	01110100 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000100 | full displacement	7 + m or 3	7 + m or 3		r
JNE/JNZ = Jump on Not Equal/Not Zero					
8-Bit Displacement	01110101 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000101 | full displacement	7 + m or 3	7 + m or 3		r
JBE/JNA = Jump on Below or Equal/Not Above					
8-Bit Displacement	01110110 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000110 | full displacement	7 + m or 3	7 + m or 3		r
JNBE/JA = Jump on Not Below or Equal/Above					
8-Bit Displacement	01110111 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10000111 | full displacement	7 + m or 3	7 + m or 3		r
JS = Jump on Sign					
8-Bit Displacement	01111000 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001000 | full displacement	7 + m or 3	7 + m or 3		r

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
CONDITIONAL JUMPS (Continued)					
JNS = Jump on Not Sign					
8-Bit Displacement	01111001 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001001 | full displacement	7 + m or 3	7 + m or 3		r
JP/JPE = Jump on Parity/Parity Even					
8-Bit Displacement	01111010 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001010 | full displacement	7 + m or 3	7 + m or 3		r
JNP/JPO = Jump on Not Parity/Parity Odd					
8-Bit Displacement	01111011 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001011 | full displacement	7 + m or 3	7 + m or 3		r
JL/JNGE = Jump on Less/Not Greater or Equal					
8-Bit Displacement	01111100 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001100 | full displacement	7 + m or 3	7 + m or 3		r
JNL/JGE = Jump on Not Less/Greater or Equal					
8-Bit Displacement	01111101 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001101 | full displacement	7 + m or 3	7 + m or 3		r
JLE/JNG = Jump on Less or Equal/Not Greater					
8-Bit Displacement	01111110 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001110 | full displacement	7 + m or 3	7 + m or 3		r
JNLE/JG = Jump on Not Less or Equal/Greater					
8-Bit Displacement	01111111 | 8-bit displ	7 + m or 3	7 + m or 3		r
Full Displacement	00001111 | 10001111 | full displacement	7 + m or 3	7 + m or 3		r
JCXZ = Jump on CX Zero	11100011 | 8-bit displ	9 + m or 5	9 + m or 5		r
JECXZ = Jump on ECX Zero	11100011 | 8-bit displ	9 + m or 5	9 + m or 5		r
(Address Size Prefix Differentiates JCXZ from JECXZ)					
LOOP = Loop CX Times	11100010 | 8-bit displ	11 + m	11 + m		r
LOOPZ/LOOPE = Loop with Zero/Equal	11100001 | 8-bit displ	11 + m	11 + m		r
LOOPNZ/LOOPNE = Loop While Not Zero	11100000 | 8-bit displ	11 + m	11 + m		r
CONDITIONAL BYTE SET					
NOTE: Times Are Register/Memory					
SETO = Set Byte on Overflow					
To Register/Memory	00001111 | 10010000 | mod 000 r/m	4/5	4/5		h
SETNO = Set Byte on Not Overflow					
To Register/Memory	00001111 | 10010001 | mod 000 r/m	4/5	4/5		h
SETB/SETNAE = Set Byte on Below/Not Above or Equal					
To Register/Memory	00001111 | 10010010 | mod 000 r/m	4/5	4/5		h

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
CONDITIONAL BYTE SET (Continued)					
SETNB = Set Byte on Not Below/Above or Equal					
To Register/Memory	00001111 | 10010011 | mod 000 r/m	4/5	4/5		h
SETE/SETZ = Set Byte on Equal/Zero					
To Register/Memory	00001111 | 10010100 | mod 000 r/m	4/5	4/5		h
SETNE/SETNZ = Set Byte on Not Equal/Not Zero					
To Register/Memory	00001111 | 10010101 | mod 000 r/m	4/5	4/5		h
SETBE/SETNA = Set Byte on Below or Equal/Not Above					
To Register/Memory	00001111 | 10010110 | mod 000 r/m	4/5	4/5		h
SETNBE/SETA = Set Byte on Not Below or Equal/Above					
To Register/Memory	00001111 | 10010111 | mod 000 r/m	4/5	4/5		h
SETS = Set Byte on Sign					
To Register/Memory	00001111 | 10011000 | mod 000 r/m	4/5	4/5		h
SETNS = Set Byte on Not Sign					
To Register/Memory	00001111 | 10011001 | mod 000 r/m	4/5	4/5		h
SETP/SETPE = Set Byte on Parity/Parity Even					
To Register/Memory	00001111 | 10011010 | mod 000 r/m	4/5	4/5		h
SETNP/SETPO = Set Byte on Not Parity/Parity Odd					
To Register/Memory	00001111 | 10011011 | mod 000 r/m	4/5	4/5		h
SETL/SETNGE = Set Byte on Less/Not Greater or Equal					
To Register/Memory	00001111 | 10011100 | mod 000 r/m	4/5	4/5		h
SETNL/SETGE = Set Byte on Not Less/Greater or Equal					
To Register/Memory	00001111 | 01111101 | mod 000 r/m	4/5	4/5		h
SETLE/SETNG = Set Byte on Less or Equal/Not Greater					
To Register/Memory	00001111 | 10011110 | mod 000 r/m	4/5	4/5		h
SETNLE/SETG = Set Byte on Not Less or Equal/Greater					
To Register/Memory	00001111 | 10011111 | mod 000 r/m	4/5	4/5		h
ENTER = Enter Procedure	11001000 | 16-bit displacement, 8-bit level				
L = 0		10	10	b	h
L = 1		12	12	b	h
L > 1		15 + 4(n − 1)	15 + 4(n − 1)	b	h
LEAVE = Leave Procedure	11001001	4	4	b	h

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT		NOTES	
		Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode
INTERRUPT INSTRUCTIONS					
INT = Interrupt:					
Type Specified	11001101 | type	37		b	
Type 3	11001100	33		b	
INTO = Interrupt 4 If Overflow Flag Set	11001110				
If OF = 1		35		b, e	
If OF = 0		3	3	b, e	
Bound = Interrupt 5 If Detect Value Out of Range	01100010 | mod reg r/m				
If Out of Range		44		b, e	e, g, h, j, k, r
If In Range		10	10	b, e	e, g, h, j, k, r
Protected Mode Only (INT)					
INT: Type Specified					
Via Interrupt or Trap Gate to Same Privilege Level			59		g, j, k, r
Via Interrupt or Trap Gate to Different Privilege Level			99		g, j, k, r
From 286 Task to 286 TSS via Task Gate			282		g, j, k, r
From 286 Task to 386 TSS via Task Gate			309		g, j, k, r
From 286 Task to virt 8086 md via Task Gate			226		g, j, k, r
From 386 Task to 286 TSS via Task Gate			284		g, j, k, r
From 386 Task to 386 TSS via Task Gate			311		g, j, k, r
From 386 Task to virt 8086 md via Task Gate			228		g, j, k, r
From virt 8086 md to 286 TSS via Task Gate			289		g, j, k, r
From virt 8086 md to 386 TSS via Task Gate			316		g, j, k, r
From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate			119		
INT: TYPE 3					
Via Interrupt or Trap Gate to Same Privilege Level			59		g, j, k, r
Via Interrupt or Trap Gate to Different Privilege Level			99		g, j, k, r
From 286 Task to 286 TSS via Task Gate			278		g, j, k, r
From 286 Task to 386 TSS via Task Gate			305		g, j, k, r
From 286 Task to Virt 8086 md via Task Gate			222		g, j, k, r
From 386 Task to 286 TSS via Task Gate			280		g, j, k, r
From 386 Task to 386 TSS via Task Gate			307		g, j, k, r
From 386 Task to Virt 8086 md via Task Gate			224		g, j, k, r
From virt 8086 md to 286 TSS via Task Gate			285		g, j, k, r
From virt 8086 md to 386 TSS via Task Gate			312		g, j, k, r
From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate			119		
INTO:					
Via Interrupt or Trap Gate to Same Privilege Level			59		g, j, k, r
Via Interrupt or Trap Gate to Different Privilege Level			99		g, j, k, r
From 286 Task to 286 TSS via Task Gate			280		g, j, k, r
From 286 Task to 386 TSS via Task Gate			307		g, j, k, r
From 286 Task to virt 8086 md via Task Gate			224		g, j, k, r
From 386 Task to 286 TSS via Task Gate			282		g, j, k, r
From 386 Task to 386 TSS via Task Gate			309		g, j, k, r
From 386 Task to virt 8086 md via Task Gate			226		g, j, k, r
From virt 8086 md to 286 TSS via Task Gate			287		g, j, k, r
From virt 8086 md to 386 TSS via Task Gate			314		g, j, k, r
From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate			119		

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
INTERRUPT INSTRUCTIONS (Continued)					
BOUND:					
Via Interrupt or Trap Gate to Same Privilege Level			59		g, j, k, r
Via Interrupt or Trap Gate to Different Privilege Level			99		g, j, k, r
From 286 Task to 286 TSS via Task Gate			254		g, j, k, r
From 286 Task to 386 TSS via Task Gate			284		g, j, k, r
From 286 Task to virt 8086 Mode via Task Gate			231		g, j, k, r
From 386 Task to 286 TSS via Task Gate			264		g, j, k, r
From 386 Task to 386 TSS via Task Gate			294		g, j, k, r
From 386 Task to virt 8086 Mode via Task Gate			243		g, j, k, r,
From virt 8086 Mode to 286 TSS via Task Gate			264		g, j, k, r
From virt 8086 Mode to 386 TSS via Task Gate			294		g, j, k, r
From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate			119		
INTERRUPT RETURN					
IRET = Interrupt Return	11001111	22			g, h, j, k, r
Protected Mode Only (IRET)					
To the Same Privilege Level (within task)			38		g, h, j, k, r
To Different Privilege Level (within task)			82		g, h, j, k, r
From 286 Task to 286 TSS			232		h, j, k, r
From 286 Task to 386 TSS			265		h, j, k, r
From 286 Task to Virtual 8086 Task			214		h, j, k, r
From 286 Task to Virtual 8086 Mode (within task)			60		
From 386 Task to 286 TSS			271		h, j, k, r
From 386 Task to 386 TSS			275		h, j, k, r
From 386 Task to Virtual 8086 Task			224		h, j, k, r
From 386 Task to Virtual 8086 Mode (within task)			60		
PROCESSOR CONTROL					
HLT = HALT	11110100	5	5		l
MOV = Move to and From Control/Debug/Test Registers					
CR0/CR2/CR3 from register	00001111 00100010 11 eee reg	10/4/5	10/4/5		l
Register From CR0–3	00001111 00100000 11 eee reg	6	6		l
DR0–3 From Register	00001111 00100011 11 eee reg	22	22		l
DR6–7 From Register	00001111 00100011 11 eee reg	16	16		l
Register from DR6–7	00001111 00100001 11 eee reg	14	14		l
Register from DR0–3	00001111 00100001 11 eee reg	22	22		l
TR6–7 from Register	00001111 00100110 11 eee reg	12	12		l
Register from TR6–7	00001111 00100100 11 eee reg	12	12		l
NOP = No Operation	10010000	3	3		
WAIT = Wait until BUSY # pin is negated	10011011	6	6		

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
PROCESSOR EXTENSION INSTRUCTIONS					
Processor Extension Escape	11011TTT | mod LLL r/m TTT and LLL bits are opcode information for coprocessor.	See 80287/80387 data sheets for clock counts			h
PREFIX BYTES					
Address Size Prefix	01100111	0	0		
LOCK = Bus Lock Prefix	11110000	0	0		m
Operand Size Prefix	01100110	0	0		
Segment Override Prefix					
CS:	00101110	0	0		
DS:	00111110	0	0		
ES:	00100110	0	0		
FS:	01100100	0	0		
GS:	01100101	0	0		
SS:	00110110	0	0		
PROTECTION CONTROL					
ARPL = Adjust Requested Privilege Level					
From Register/Memory	01100011 | mod reg r/m	N/A	20/21	a	h
LAR = Load Access Rights					
From Register/Memory	00001111 | 00000010 | mod reg r/m	N/A	15/16	a	g, h, i, p
LGDT = Load Global Descriptor					
Table Register	00001111 | 00000001 | mod 010 r/m	11	11	b, c	h, i
LIDT = Load Interrupt Descriptor					
Table Register	00001111 | 00000001 | mod 011 r/m	11	11	b, c	h, i
LLDT = Load Local Descriptor					
Table Register to Register/Memory	00001111 | 00000000 | mod 010 r/m	N/A	20/24	a	g, h, i, l
LMSW = Load Machine Status Word					
From Register/Memory	00001111 | 00000001 | mod 110 r/m	10/13	10/13	b, c	h, i
LSL = Load Segment Limit					
From Register/Memory	00001111 | 00000011 | mod reg r/m				
Byte-Granular Limit		N/A	20/21	a	g, h, i, p
Page-Granular Limit		N/A	25/26	a	g, h, i, p
LTR = Load Task Register					
From Register/Memory	00001111 | 00000000 | mod 001 r/m	N/A	23/27	a	g, h, i, l
SGDT = Store Global Descriptor					
Table Register	00001111 | 00000001 | mod 000 r/m	9	9	b, c	h

80386 Instruction Set Clock Count Summary (Continued)

INSTRUCTION	FORMAT	CLOCK COUNT: Real Address Mode or Virtual 8086 Mode	CLOCK COUNT: Protected Virtual Address Mode	NOTES: Real Address Mode or Virtual 8086 Mode	NOTES: Protected Virtual Address Mode
SIDT – Store Interrupt Descriptor Table Register	00001111 | 00000001 | mod 001 r/m	9	9	b, c	h
SLDT – Store Local Descriptor Table Register To Register/Memory	00001111 | 00000000 | mod 000 r/m	N/A	2/2	a	h
SMSW – Store Machine Status Word	00001111 | 00000001 | mod 100 r/m	10/13	10/13	b, c	h, l
STR – Store Task Register To Register/Memory	00001111 | 00000000 | mod 001 r/m	N/A	2/2	a	h
VERR – Verify Read Access Register/Memory	00001111 | 00000000 | mod 100 r/m	N/A	10/11	a	g, h, j, p
VERW – Verify Write Access	00001111 | 00000000 | mod 101 r/m	N/A	15/16	a	g, h, j, p

INSTRUCTION NOTES FOR TABLE 8-1

Notes a through c apply to 80386 Real Address Mode only:

a. This is a Protected Mode instruction. Attempted execution in Real Mode will result in exception 6 (invalid opcode).

b. Exception 13 fault (general protection) will occur in Real Mode if an operand reference is made that partially or fully extends beyond the maximum CS, DS, ES, FS or GS limit, FFFFH. Exception 12 fault (stack segment limit violation or not present) will occur in Real Mode if an operand reference is made that partially or fully extends beyond the maximum SS limit.

c. This instruction may be executed in Real Mode. In Real Mode, its purpose is primarily to initialize the CPU for Protected Mode.

Notes d through g apply to 80386 Real Address Mode and 80386 Protected Virtual Address Mode:

d. The 80386 uses an early-out multiply algorithm. The actual number of clocks depends on the position of the most significant bit in the operand (multiplier).

Clock counts given are minimum to maximum. To calculate actual clocks use the following formula:

Actual Clock = if m < > 0 then max ($[\log_2 |m|]$, 3) + 6 clocks:
if m = 0 then 9 clocks (where m is the multiplier)

e. An exception may occur, depending on the value of the operand.

f. LOCK# is automatically asserted, regardless of the presence or absence of the LOCK# prefix.

g. LOCK# is asserted during descriptor table accesses.

Notes h through r apply to 80386 Protected Virtual Address Mode only:

h. Exception 13 fault (general protection violation) will occur if the memory operand in CS, DS, ES, FS or GS cannot be used due to either a segment limit violation or access rights violation. If a stack limit is violated, an exception 12 (stack segment limit violation or not present) occurs.

i. For segment load operations, the CPL, RPL, and DPL must agree with the privilege rules to avoid an exception 13 fault (general protection violation). The segment's descriptor must indicate "present" or exception 11 (CS, DS, ES, FS, GS not present). If the SS register is loaded and a stack segment not present is detected, an exception 12 (stack segment limit violation or not present) occurs.

j. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert LOCK# to maintain descriptor integrity in multiprocessor systems.

k. JMP, CALL, INT, RET and IRET instructions referring to another code segment will cause an exception 13 (general protection violation) if an applicable privilege rule is violated.

l. An exception 13 fault occurs if CPL is greater than 0 (0 is the most privileged level).

m. An exception 13 fault occurs if CPL is greater than IOPL.

n. The IF bit of the flag register is not updated if CPL is greater than IOPL. The IOPL and VM fields of the flag register are updated only if CPL = 0.

o. The PE bit of the MSW (CR0) cannot be reset by this instruction. Use MOV into CR0 if desiring to reset the PE bit.

p. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the zero flag is cleared.

q. If the coprocessor's memory operand violates a segment limit or segment access rights, an exception 13 fault (general protection exception) will occur before the ESC instruction is executed. An exception 12 fault (stack segment limit violation or not present) will occur if the stack limit is violated by the operand's starting address.

r. The destination of a JMP, CALL, INT, RET or IRET must be in the defined limit of a code segment or an exception 13 fault (general protection violation) will occur.

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