International Technical Assistance BULLETIN

Augsburg, August 31, 1971 No. G-159-71

TO ALL INTERNATIONAL TECHNICAL SERVICE MANAGERS AND CLASS 446 TECHNICIANS:

NEW CLASS 446 WITH STANDARD LOGIC

12 or 48 Totals

This Bulletin contains a technical description of the new 12 or 48-total Class 446 systems with the so called "standard logic". It is intended for familiarizing a trained Class 446 technician with the differences between the new and the previous systems. This should allow him to service the new models without the need of attending an additional training course.

The following references will be required for the explanations given below: the Class 446 Service Manual MS-5020 and the International Technical Assistance Bulletins No. G-151-71, G-154-71, and G-158-71.

Whenever possible, a 48-total Class 446 system should be available as a practical aid in the study.

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F-2539-OE-Dayton - 8-1-68 - The NCR Co. printed in Germany

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1. GENERAL INFORMATION

The core logic of Class 446 "prepared for peripherals" models has been redesigned with the following objectives:

- to reduce the number of differing core logic types from 4 to 2;
- to allow an increase in the storage capacity from 12 to 48 totals;
- to allow a conversion of 12-total models to 48-total models.

At the same time, certain logic changes will increase the operating convenience and reliability:

A. The PPK command will include:

- an automatic release of the Printer, Data & Function Keyboards;
- automatic locking of the Printer Keyboard when PPK is terminated.

B. An overlapping input cannot influence the Punch Buffer reset any more.

C. For reading the logic cores, a full current of 460 mA will be used instead of two half-currents of 230 mA each.

Compared with the previous "prepared for peripherals" models, the following features have been added to the new models:

A. Any of the 48 totals can be selected:

- directly, through an n1 or n2 address (as before);
- indirectly, through a modified n1 or n2 address.

B. The number of Skip Programs has been increased from 10 to 16 (Skip 0 to 15).

C. The Skip Programs and Subprograms can be selected by two new program instructions.

In addition to a number of minor electronic changes, the 48-total model had to be provided with an additional plug-in board in location 1L. This board comprises the following circuits:

- Storage plane selection circuit (4 planes with 12 storage registers each)
- indirect total selection circuit.

1.1 Model Information Chart

Models listed under A1 and A3 are supplied with 12-total capacity. They can be converted to 48 totals by using the Electronics Unit Retro-fit Kit F01 (800-0008400). The installation instructions are attached to the parts kit.

	Electronics Unit Model No.	Core Logic Assy Part No.
A. New Models		
1. Standard Decimal "prepared for 48 storages"	446-507-03-12	800-0006209
2. Standard Decimal "with 48 storages"	446-508-03-48	800-0006209
3. Standard Katakana "prepared for 48 storages"	446-509-04-12	800-0006210
4. Standard Katakana "with 48 storages"	446-510-04-48	800-0006210
B. Discontinued Models		
1. "Prepared for Peripherals with 48 storages" *	446-519-03-48	800-0006207
2. "Prepared for Peripherals", Decimal	446-509-03-12	800-0006203
3. "Prepared for Peripherals", Sweden	446-512-04-12	800-0006204
4. "Prepared for Peripherals", Sterling	446-518-06-12	800-0006206
5. "Prepared for Peripherals", Katakana	446-515-05-12	800-0006205
C. Still available, unchanged Models:		
1. Basic, Decimal	446-503-01-12	800-0006201
2. Basic, Sweden	446-506-02-12	800-0006202

* This so called "Transient Model" was supplied only to a few countries. A technical explanation of this model was provided as a Circular Letter dated June 1, 1971 to the countries concerned.

1.2 Test Programs

New service test tapes have been developed for the standard logic models. They can be ordered from the Technical Service Managers.

The changed HLT code makes the previous test tapes incompatible.

Test Tapes	Designation
Internal Reliability Test (for 12-total models)	"CORE 12"
Internal Reliability Test (for 48-total models)	"CORE 48"
Printer Test	"P-48"
Reader A & B and Punch Test	"A + B 48"

The "P48" and "A+B 48" tapes are compatible with both 12- and 48-logic models.

The test tape required for electronics adjustments by the mean-value method is coded at the end of all test tapes listed above. Its designation is:

"E-ADJ 48" for the 48-total model,
"E-ADJ 12" for all 12-total models.

The "E-ADJ 12" tape replaces the "E-ADJ O.S." tape described in ITAB No. G-151-71. The "E-ADJ O.S." tape cannot be used for adjusting the 12-total standard-logic models.

Coding instructions for these new test programs will be published at a later date.

1.3 Additional Components

The standard-logic models have been provided with the following new parts:

Plug-in Board, Printer Control I		800-0005490
Plug-in Board, Storage Selection	(48 totals)	800-0005455
Plug-in Board, PR-PL Gates	(12 totals)	800-0005480
Plug-in Board, PR-PL Gates	(48 totals)	800-0005445
Fuse, 30 A		800-0082092

For core logic part numbers refer to the Model Information Chart above (Item 1.1).

2. DIFFERENCES FROM PREVIOUS MODELS

The differences and changes in the electronics and in the programing, as described in this section, apply to both 12 and 48-total standard-logic models. The specific changes applicable to the 48-total model only are described in section 3.

2.1 Electronics

2.1.1 Final Stage (Full Logic Read Current)

Instead of the previous two half-currents of 230 mA each used for reading the logic cores, one full read current of 460 mA is now used. The necessary changes in the CC Final Stage circuit design can be seen by comparing Fig. 8-2 in the Class 446 Service Manual with Fig. 2-1 below.

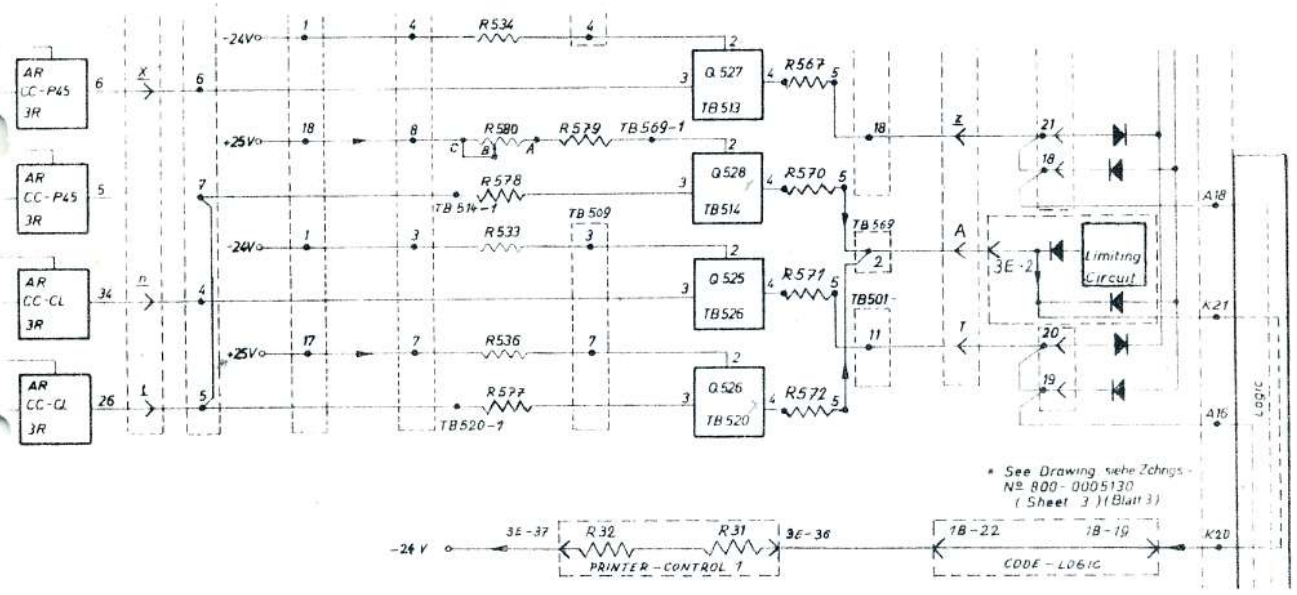


Fig. 2-1

As a result of this change, the two CC-final stage transistors Q526 and Q528 will be controlled at C3 time by one Gate only (Pin 3 R26). The current rise to the required read level will be smoother than in the previous design. This will increase the reliability of logic core read operations.

The common logic driver wire is threaded through all logic cores including the code logic cores. Similar to the Inhibit circuit, the reliability of the driver circuit has been improved by:

- increasing its voltage to 49 V (+25 V to -24 V);
- adding a limiter circuit to limit the noise voltage.

NOTE: For this reason, the Printer Control I and Code Logic boards of the previous models cannot be used for the standard logic models. See Fig. 2-1.

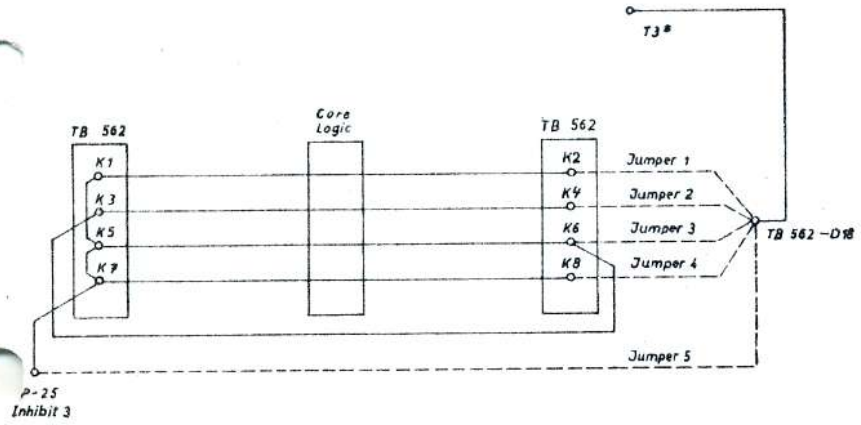
Adjustments

The read current level passing through transistor Q526 should be adjusted, as before, to 230 mA using Potentiometer R45. Next, the current passing Q528 should be adjusted with the new Potentiometer R580 to 230 mA. R580 is located in the right upper part of the Final Stage Panel.

2.1.2 No. 3 Inhibit

The signs "%", "‰", Decimal Point and Minus (-) can be selected by the core logic during an OFS operation. Refer to page 9-133 and 13-5 in the Class 446 Service Manual.

The "per cent" (%), decimal point (.) and minus (-) signs have different locations on the print heads for some countries. To accomplish correct selection of these signs, a corresponding part of the core logic is selected by means of jumper connections. See Jumpers 1 to 5 in Fig. 2-2.



Jumper No.	Model No. of Console
1	446-xxx-201 thru 204
2	446-xxx-206*
3	446-xxx-206*
4	446-xxx-205
5	446-xxx-207

*Two different Printheads can be used in this model.

Fig. 2-2

2.1.3 Power Supply

To each of the 3 final stages of the +12 volt supply one more transistor NCR 8-05 has been added. Compare Fig. 2-3 below with Fig. 6-55A in the Service Manual.

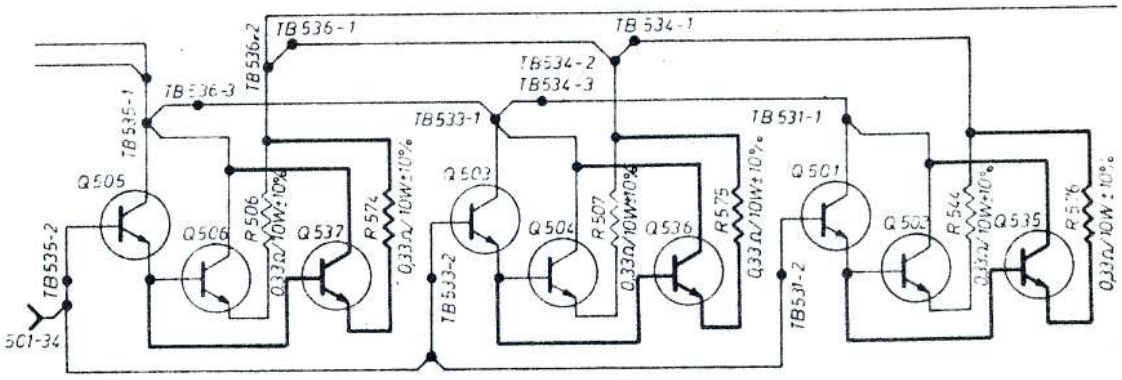


Fig. 2-3

2.1.4 CC Control I

By increasing Capacitor C7 from 470 pF to 1000 pF the CCR rise time has been increased allowing a wider operating range of the Strobe. Refer to ITAB No. G-151-71, page 8.

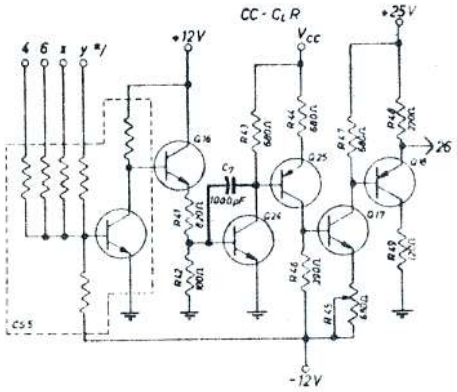


Fig. 2-4

2.2 Programming

The programs designed for the previous models are not compatible with the new standard-logic models. See Item 2.2.1. For new program codes see Item 3.2.4.

2.2.1 HLT Code

Since channel 6 is reserved for plane selection in the 48-total model, the HLT symbol cannot be punched together with an n1 address any more. Its code had to be changed as follows:

	Previous Models		New Models	
1st column	X0	T6	HLT	T5T6T7
2nd column	IFC	T2T3	0	
3rd column	0		IFC	T2T3
4th column			0	

2.2.2 LFE Code

The Line Finder Eject (LFE) code has been changed from 30 to 62 by adding a hole in channel 6. Thus the core logic will treat LFE like any other printer operation. See ITAB No. G-158-71 and Fig. 9-11 in the Service Manual.

2.2.3 Additional PPK Features

A change in the core logic extends the PPK command to effect:

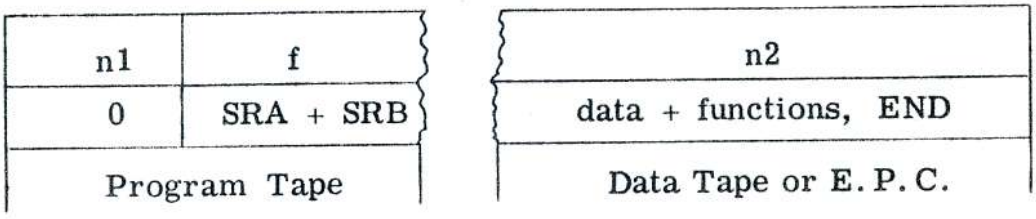
- an automatic release of the Printer, Data and Function keyboards;
- automatic locking of all keyboards upon the termination of PPK (with the AB key depressed);
- automatic locking of the printer keyboard when the "Field Length" programed in the n1 address has been reached. See page 3-15 in the Service Manual.

These extended functions of PPK supersede the delayed release of the Printer Keyboard described in ITAB No. G-154-71.

2.2.4 Skip, Reader A or B

Two new commands - SRA and SRB - allow skipping an n2 address on a data tape or edge-punched card.

The codes for SRA and SRB differ from the ORA and ORB codes by an added hole in channel 1.



The data in the n2 address will be read up to the END symbol, however they will be neither printed nor punched as on ORA or ORB. See page 3-16 in the Service Manual.

NOTE: No core logic change was required for adding the commands SRA and SRB.

The channel 1 hole will set up the condition H25 H26/ in PC64.

H25 = print suppression;

H26/ = Punch suppression. See page 13-4 in the Service Manual.

3. 48-TOTAL MODEL

The changes in the electronics and the programming, as described in Section 2, apply also to the 48-total models.

3.1 Electronics Functions

Whenever possible, a 48-total model should be made available to the student to increase the effectiveness of the study.

3.1.1 Added Storage Capacity

The 48 Storage Registers are arranged in 4 Storage Planes, each one consisting of 12 registers. Full read and write current will be applied only to the 12 Registers in a plane selected by the program.

The number of PR Gates has been increased from 4 to 16, with 4 PR Gates assigned to each Storage Plane. See Fig. 3-1. To access a Storage Plane, a group of 4 PR Gates must be selected.

The P Gates (P1 to P12) are common to all Storage Planes. Compare Fig. 3-1 below with Fig. 7-1 in the Class 446 Service Manual. Each register core of the 48 Registers will receive one CCR-CCW half-current through Power Gates P1 to P12. The second half-current will be applied through the selected group of PR Gates.

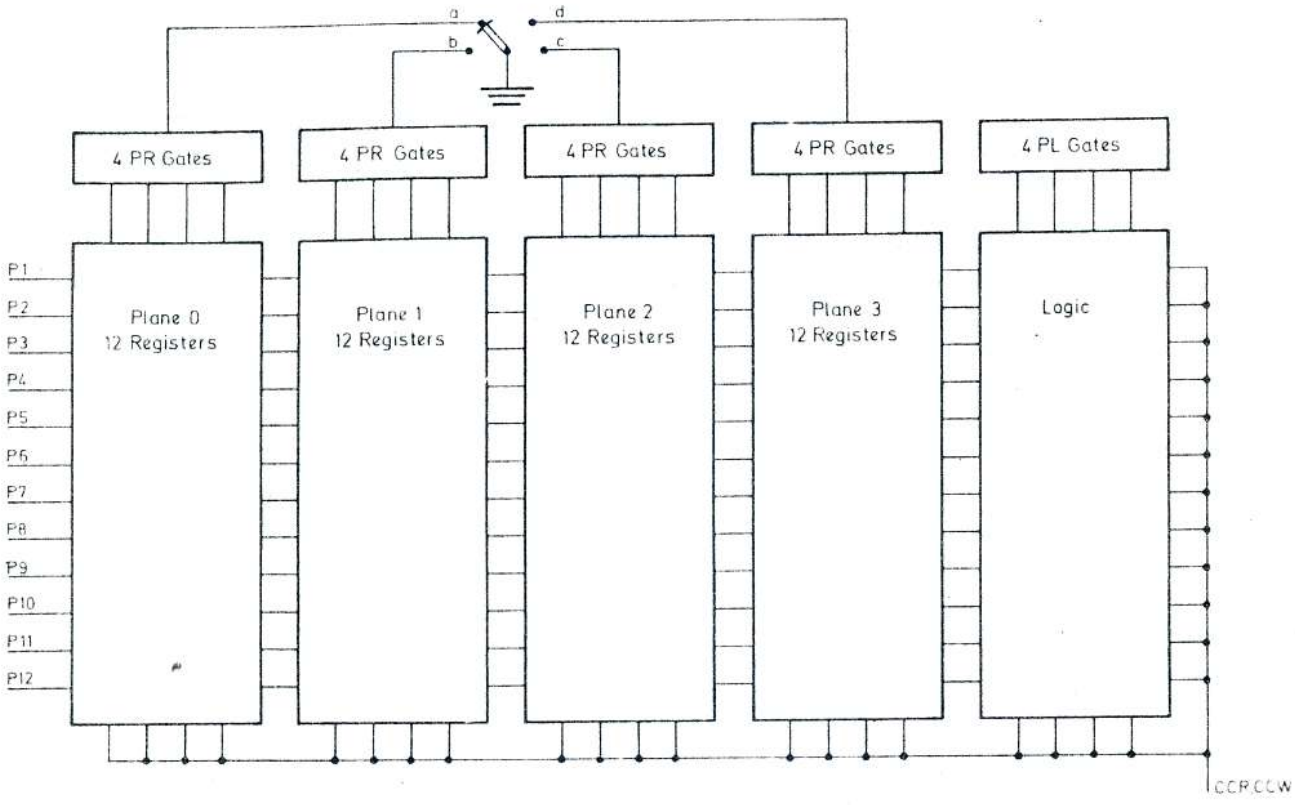


Fig. 3-1

Fig. 3-2 shows the new designations of the PR Gates and the addressing of registers.

Note that the second digit of each Gate No. is the same as that of the corresponding Plane.

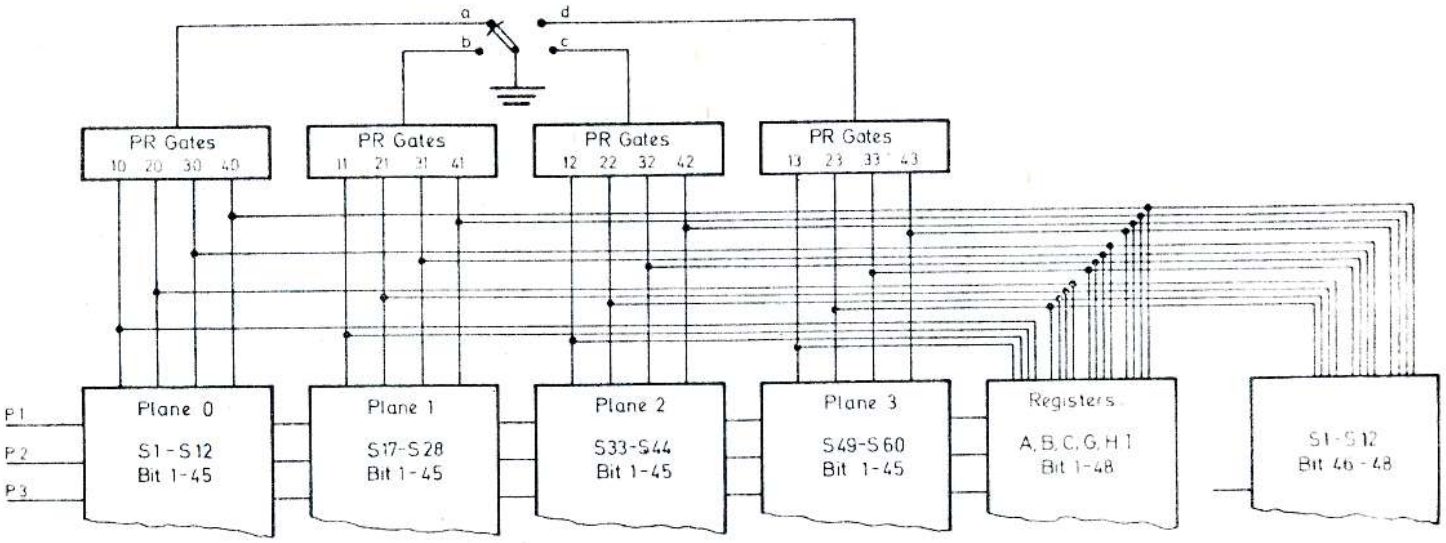


Fig. 3-2

The 48 register cores of the Working Registers (A, B, C, G, H, & I) are wired to receive full Read/Write currents regardless of the Storage Plane selected. This applies also to the register cores which are related to the core logic, bits 46, 47, and 48 of Registers S1 to S12.

The gaps in the numerical sequence of the register addresses are assigned to the programmable working registers C (13), B (14), I (15), and H (16). These Working Registers are common to all Storage Planes (therefore the addresses 29 to 32 and 45 to 48 cannot be used as register addresses).

Since only one Storage Plane can be abled at a time, the existing 12 Sense Amplifiers and the 12 Transfer Circuits for Registers S1-S12 are sufficient for all 4 Storage Planes.

The Sense Wire of Sense Amplifier S1 is threaded through all cores of the first register in each of the 4 Storage Planes (S1, S17, S33, S49). The sense wire of Sense Amplifier S2 is threaded through all the cores of the second register in each Storage Plane (S2, S18, S34, S50) etc. The same applies to the Inhibit Wires.

3.1.2 Storage Plane Selection

The four Storage Planes are selected from channels 5 and 6 of the program tape:

Storage Plane 0: no holes in channels 5 and 6;

Storage Plane 1: a hole in channel 5;

Storage Plane 2: a hole in channel 6;

Storage Plane 3: holes in channels 5 and 6.

The Photo Amplifier outputs of channels 5 and 6 (V5 and V6) are applied to a Plane Selection Control Circuit on the additional Plug-in Board in location 1L. See Fig. 3.3.

The 4 possible configurations of V5 and V6 cause one of the four outputs a, b, c, or d to be set to 0 V. See the Truth Table below.

V5	V6	a	b	c	d	
0	0	0	1	1	1	Plane 0
1	0	1	0	1	1	Plane 1
0	1	1	1	0	1	Plane 2
1	1	1	1	1	0	Plane 3

The transfer to a different Storage Plane occurs in two steps:

- bit 47 time: Plane 0 will be selected automatically;
- bit 48 time: the new Plane will be selected.

To avoid possible interference with CCR and CCW currents during register times C1 and C4, these transfers take place during the logic time C2 when PR Gates are inactive.

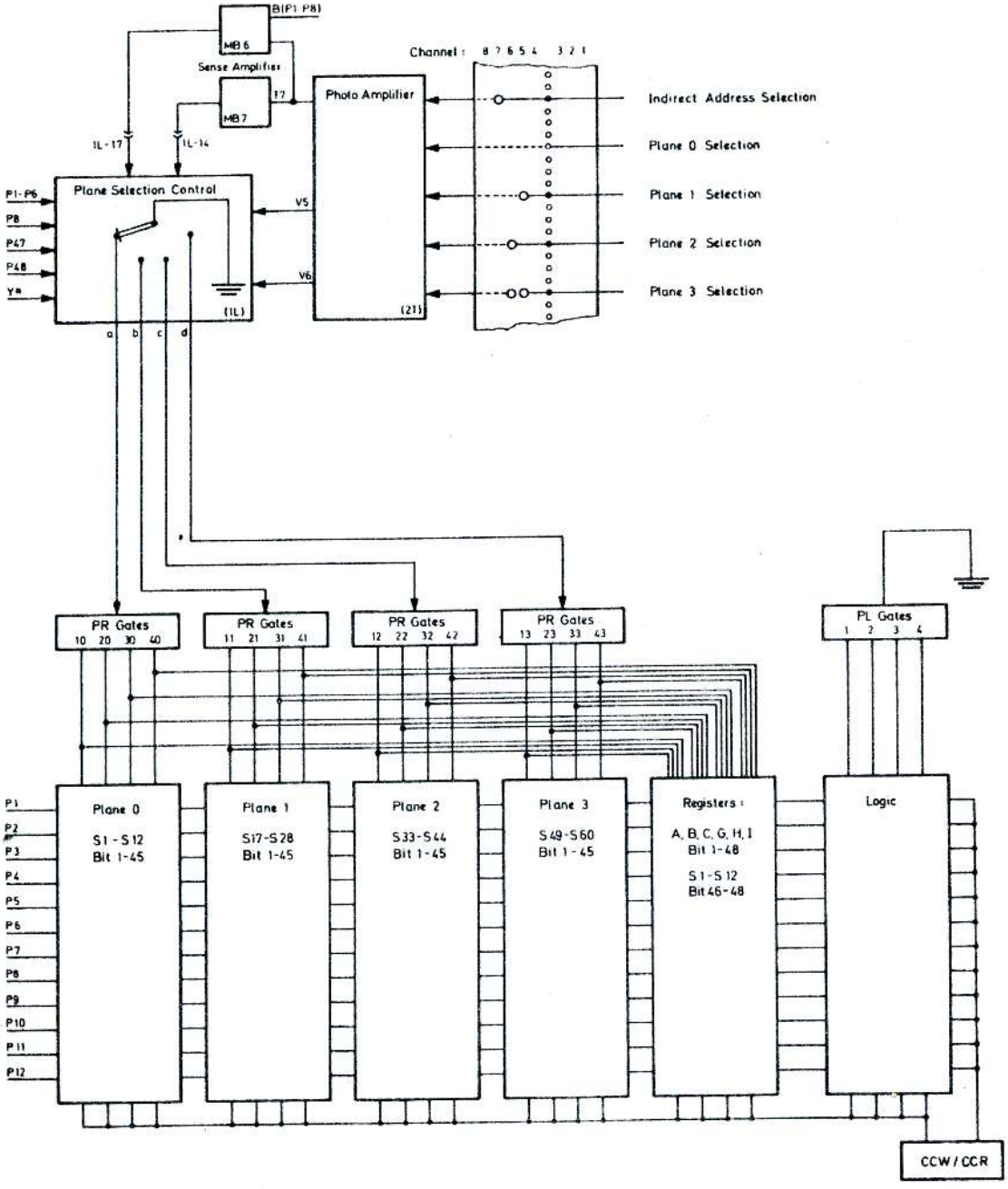

B(P1 P8)
MB 6
Sense Amplifier
MB 7
17
Photo Amplifier
Channel : 8 7 6 5 4 3 2 1
Indirect Address Selection
Plane 0 Selection
Plane 1 Selection
Plane 2 Selection
Plane 3 Selection
IL-17
IL-14
Plane Selection Control
P1-P6
P8
P47
P48
Y=
V5
V6
(IL)
(21)
a
b
c
d
PR Gates
10 20 30 40
PR Gates
11 21 31 41
PR Gates
12 22 32 42
PR Gates
13 23 33 43
PL Gates
1 2 3 4
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
Plane 0
S1 - S12
Bit 1-45
Plane 1
S17-S28
Bit 1-45
Plane 2
S33-S44
Bit 1-45
Plane 3
S49-S60
Bit 1-45
Registers :
A, B, C, G, H, I
Bit 1-48
S1-S12
Bit 46-48
Logic
CCW / CCR

Fig. 3-3

3.1.3 Storage Plane Selection Sequence

Whenever a different configuration of holes in channels 5 and 6 is read in, another Storage Plane is selected. This occurs even if it is not required by the program sequence, as when the n2 address of OFP is read in.

The selection of the new plane is initiated by the signal T1-T9 Reset. This signal exists at the start of the TSS operation (SSP, SSA, SSB) and is limited in its duration by PTL 12 and PTL 13. See figures 10-4 and 10-6 in the Class 446 Service Manual.

At the end of the PTL 13 time, Transfer Circuits T1-T8 will be set according to the holes above the photo cells. See Fig. 8-12 in the Class 446 Service Manual.

Flip flops FF3 and FF4 will, at this time, be set by V5/ and V6/ (set inputs of Transfer Circuits T5 and T6) according to the hole configuration in channels 5 and 6. See Fig. 3-5 and 3-6.

At the end of PTL 12 time this operation is completed and the tape will advance.

At the same time, flip flop FF2 was transferred by the T1-T9 Reset applied through Diode CR13 allowing flip flops FF5 and FF6 to be set during logic time C2 of bit 47.

With FF5 and FF6 set, output "a" of diode matrix CR3 thru CR10 goes to 0 volts.

With output "a" at 0 volt and outputs "b", "c", and "d" at +12 volts, the read and write currents (CCR, CCW) will pass through PR Gates 10, 20, 30, and 40. The Storage Plane 0, S1 to S12, will be selected at bit 47 time.

At the beginning of C2 time of bit 48, the hole configuration stored in flip flops FF4 and FF3 is transferred to flip flops FF5 and FF6. Outputs a, b, c, and d will be set accordingly. See the following truth table.

Channel 5	Channel 6	FF 5	FF 6	Output a b c d	Storage Plane
0	0	~~0~~	~~0~~	0 1 1 1	0
1	0	1	0	1 0 1 1	1
0	1	0	1	1 1 0 1	2
1	1	1	1	1 1 1 0	3

Depending on which PR Gate group is abled, the associated storage plane is accessed for the following bit 1 thru bit 47 times.

3.1.4 Indirect Address Selection

This new programming feature is applicable to those commands only which contain a register address in n1 or n2, such as ADD, SUB, CPY, etc.

In an indirect address selection, the contents of the n1 and/or n2 register will be the address of the required register. Indirect address selection occurs, when the n1 and/or n2 address of the command includes an additional hole in channel 7. This channel 7 modifier is represented by an X in the n1 and n2 column of the examples below.

Example 1: Direct Address Selection

S5 content:	39					
S3 content:	1					
Program:	S5	ADD	S3			
Punched Channels:	1 and 3		1 and 2			
Result:	39	+	1	=	40	

Example 2: Indirect Address Selection by n1

S5 content:	39					
S3 content:	1					
S39 content:	4					
Program:	XS5	ADD	S3			
Punched Channels:	1, 3 and 7		1 and 2			
Result:	4	+	1	=	5	

Example 3: Indirect Address Selection by n1 and n2

S5 content:	39					
S3 content:	1					
S39 content:	4					
S1 content:	10					
Program:	XS5	ADD	XS3			
Punched Channels:	1, 3 and 7		1, 2 and 7			
Result:	4	+	10	=	14	

3.1.5 Indirect Address Selection Sequence

The n1 address is read in by TSS during PC0 or PC1, while the n2 is read in during PC64. See Fig. 9-5 in the Class 446 Service Manual.

The contents of the register indicated in n1 and/or n2 will be transferred into Working Register B. See Logic Equations of PC80 (n1) and PC82 (n2). If n1 and/or n2 contains a hole in channel 7, it will be detected by the core logic (2 additional PC's). Sense Amplifier MB7 passes it to the circuit on the additional Plug-in Board in location 1L. See Fig. 3-4.

Through Sense Amplifier MB6, the Plane Selection Control Circuit receives the binary coded contents of Register B.

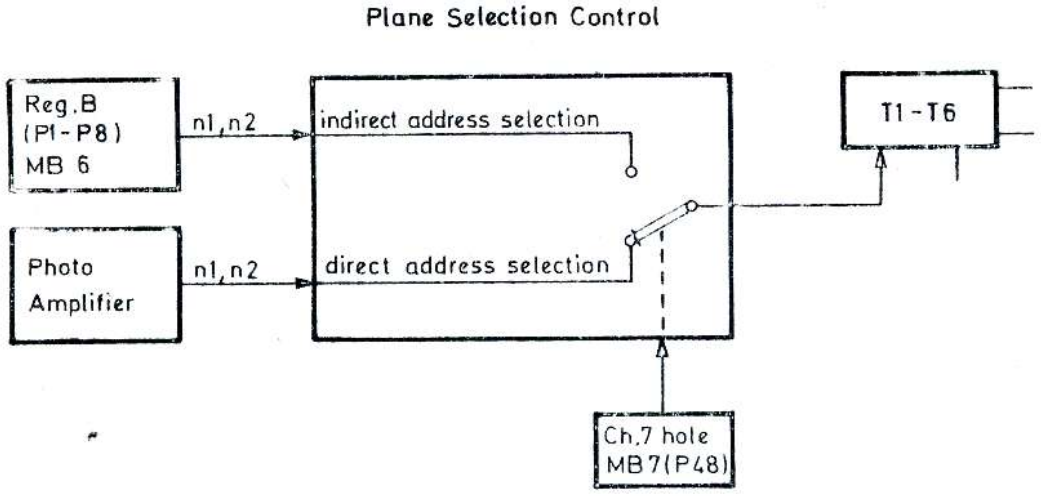


Fig. 3-4

Example:

Address n1 or n2, which was read in, contained a hole in channels 1 and 3 = S5 and an additional hole in channel 7. Register S5 contains the number 26 to select Register S26.

This number 26 will be copied in Register B to transfer the MB6 output at bit times 2, 4, and 5 (2 + 8 + 16 = 26).

The MB7 signal is generated at bit 48 time causing the following in the Plane Selection Control Circuit:

- resetting Transfer Circuits T1-T9 through diode CR22;
- transferring flip flop FF1.

See Fig. 3-5 and 3-6.

With FF1 transferred, the contents of Register B (MB6) can be passed through the Selection Gates to the set inputs of Transfer Circuits T1-T6.

The timing gate outputs cause the MB6 output to be applied to Transfer Circuits T1-T6 at proper bit times.

MB6 transfers at bit 2, 4, and 5 times.

Timing Gates LP2, LP4, and LP5 will, at the proper C3 logic time, turn on:

- Transfer Circuit T2 at bit 2 time,
- Transfer Circuit T4 at bit 4 time, and
- Transfer Circuit T5 at bit 5 time.

Together with Transfer Circuit T5, flip flop FF4, which prepares the selection of the new storage plane, will be transferred.

At the next bit 8 time:

- Transfer Circuit T9 will be set through Diode CR12;
- Flip flop FF2 will be transferred through Diode CR14:

During the next bit 47 time, the previous storage plane selection, stored in FF5 and FF6, will be reset.

At the following bit 48 time, depending on the configuration of FF4 and FF3, storage plane 1 will be selected as required for register S26.

Flow Chart

This Flow Chart shows, step by step, the operation of the Storage Plane Selection and of the Indirect Address Selection.

This method of representation offers the following advantages over a mere description:

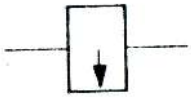
- During study:

Easier and clearer understanding of complex sequences in electronic and logic circuits, since there is no need to keep in mind the preceding steps. Each of the preceding steps and their functions is available for reference at a glance.

- During checks with a scope:

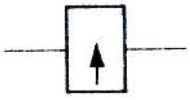
The indication of the card locations and designations of pins and components helps determine the proper test points. The references to the bit times and the representation of the actual flow sequences simplify the determination of an optimum trigger signal.

Explanation of the Flow Chart Symbols

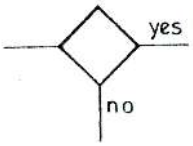
1. 

The output of the Gate indicated in the rectangular box turns to logic level "0" (approximately 0 volt).

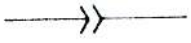
The reference output of the indicated FF turns to logic level "0" (approximately 0 volt).

2. 

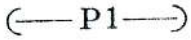
Same as above, but the outputs turn to logic level "1" (approximately +12 volts).

3. 

A diamond-shaped decision box is used when the sequence is dependent on an electronic condition or timing. If the condition is met, the sequence is continued by the line marked "yes"; if not, the "no" exit leads to the next step.

4. 

Plug-in board connector.

5. 

Steps under this symbol occur at the indicated bit time. Bit 1 in the example.

6. Ⓐ Ⓑ etc.

Start or end of a complete sequence or connection between individual segments of the entire sequence.

7. - - - - -

Dotted lines and symbols indicate an operation which does not directly affect the entire sequence.

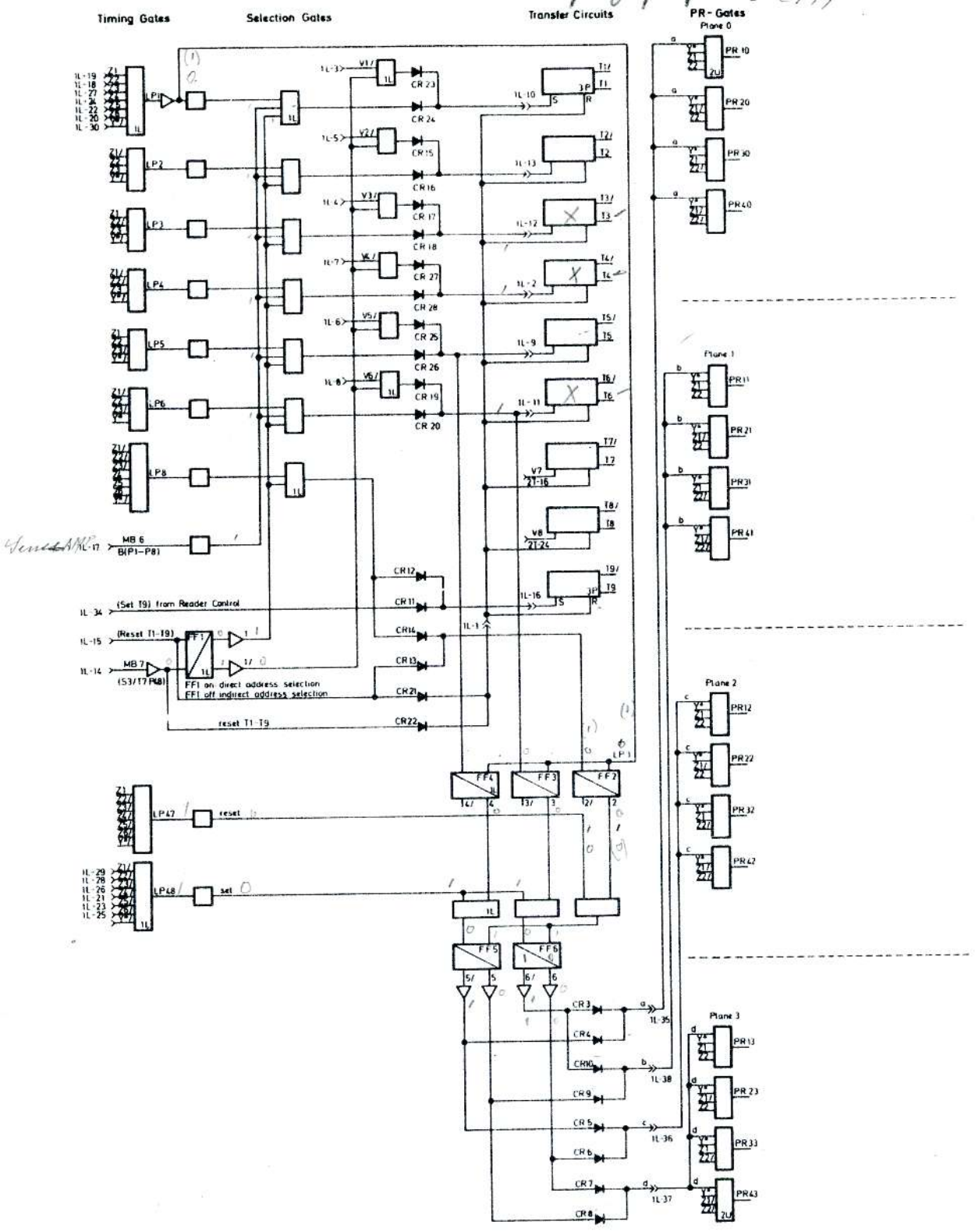


Fig. 3-6

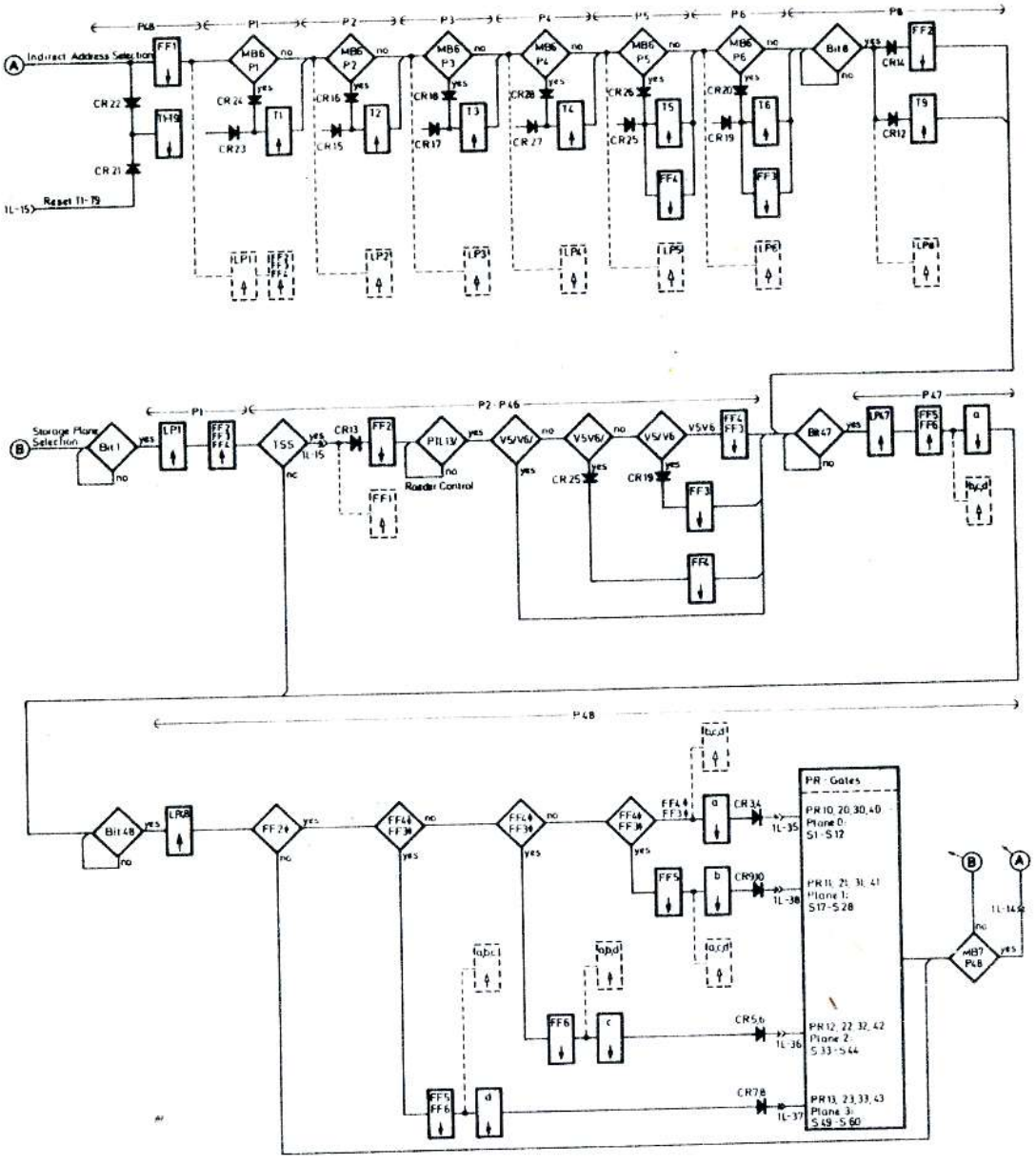

Indirect Address Selection
Reset T1-T9
Storage Plane Selection
Raster Control
PR - Gates
PR10, 20, 30, 40
Plane 0:
S1 - S12
PR11, 21, 31, 41
Plane 1:
S17 - S28
PR12, 22, 32, 42
Plane 2:
S33 - S44
PR13, 23, 33, 43
Plane 3:
S49 - S60

Fig. 3-5

3.2 Programming

The programming instructions described in Section 3 of the Class 446 Service Manual are applicable to the 48-total models. Changes and additions are described below.

The programming changes described in Item 2.2 are applicable to the 48-total models as well.

3.2.1 Added Storage Capacity

For the following commands, the n1 and n2 addresses have been extended from S1-S12 to S1-S12, S17-S28, S33-S44, and S49-S60:

ADD, SUB, MLT, DIV, and CPY

For the following commands, the n1 address only has been extended as above:

CFM, RSH, SHF, SDP, OFS, OFS1, OFS2, OFS3, OFS4, BSA, BSB, and PPK.

Refer to the chart in item 3.2.4 (under "ADDRESSES") for coding of this extended range.

Channels 1 thru 4 will be used to select a storage register within an individual plane, channels 5 and 6 to select a storage plane.

Since the Working Registers C (13), B (14), I (15) and H (16) must be accessible independently of the selected storage plane, the numerical sequence of storage addresses is interrupted by gaps. It is not allowed to use the addresses 29-32 and 45-48.

NOTE: If these addresses are nevertheless used, a working register will be selected:

- S29 or S45 will select Working Register C (13);
- S30 or S46 will select Working Register B (14), etc.

The commands listed above do not change the contents of Registers S1 to S12, S17 to S28, S33 to S44, S49 to S60, H and I. Only the CPY command modifies the contents of the register indicated in n2.

3.2.2 Indirect Address Selection

Channel 7 of the n1 and/or n2 address is used for indirect address selection. To identify such modified addresses, an X is prefixed, e.g. XS33. With channel 7 punched, the contents of the register called in n1 and/or n2 will be the address of the required register. The contents of this register in n1 and/or n2 must therefore correspond to a storage register number (1-12, 17-28, 33-44, 49-60) or a working register address (13-16). See Note in Item 3.2.1.

Channel 7 has the decimal weight of 64. This amount must be added to the storage register number when the program is punched.

Example: To program n1 = XS33, index 97 i.e. 33 + 64.

3.2.3 Indirect Subprogram and Skip Selection

Skips and Subprograms can be selected by means of two new commands, SKA and SPA.

The program tape is fed to the subprogram (using SPA), or to the skip field (using SKA), as indicated by the contents of the register which is programmed in n1.

n1	f	n2	
0, B, C, I, H, S1-S12, S17-S28, S33-S44, S49-S60	SKA	0	END

Skip Access

n1	f	n2	
0, B, C, I, H, S1-S12, S17-S28, S33-S44, S49-S60	SPA	0	END

Subprogram Access

An overflow is indicated when the contents of the n1 register:

- exceed 15,
- are negative,
- contain a decimal point.

The storage register contents are not effected.

NOTE: Skips 10 to 15 can be selected only by using SKA and not from the Function Keyboard.

3.2.4 Program Codes

The following chart completes the Class 446 program codes given in Fig. 3-18 of the Class 446 Service Manual.

ADDRESSES

1	2	3	4	5	6	7	8			Plane	Code
x								Storage	S1	0	1
	x								S2	0	2
x	x								S3	0	3
		x							S4	0	4
x		x							S5	0	5
	x	x							S6	0	6
x	x	x							S7	0	7
			x						S8	0	8
x			x						S9	0	9
	x		x						S10	0	10
x	x		x						S11	0	11
		x	x						S12	0	12
x		x	x					Register	C		13
	x	x	x					Register	B		14
x	x	x	x					Register	I		15
				x				Storage	H		16

1	2	3	4	5	6	7	8			Plane	Code
x					x			Storage	S33	2	33
	x				x				S34	2	34
x	x				x				S35	2	35
		x			x				S36	2	36
x		x			x				S37	2	37
	x	x			x				S38	2	38
x	x	x			x				S39	2	39
			x		x				S40	2	40
x			x		x				S41	2	41
	x		x		x				S42	2	42
x	x		x		x				S43	2	43
		x	x		x				S44	2	44

1	2	3	4	5	6	7	8			Plane	Code
x				x				Storage	S17	1	17
	x			x					S18	1	18
x	x			x					S19	1	19
		x		x					S20	1	20
x		x		x					S21	1	21
	x	x		x					S22	1	22
x	x	x		x					S23	1	23
			x	x					S24	1	24
x			x						S25	1	25
	x		x						S26	1	26
x	x		x						S27	1	27
		x	x						S28	1	28

1	2	3	4	5	6	7	8			Plane	Code
x					x	x		Storage	S49	3	49
	x				x	x			S50	3	50
x	x				x	x			S51	3	51
		x			x	x			S52	3	52
x		x			x	x			S53	3	53
	x	x			x	x			S54	3	54
x	x	x			x	x			S55	3	55
			x	x	x				S56	3	56
x			x		x	x			S57	3	57
	x		x		x	x			S58	3	58
x	x		x		x	x			S59	3	59
		x	x		x	x			S60	3	60

COMMANDS

1	2	3	4	5	6	7	8		Code
	x	x	x	x	x	x		SKA	126
x	x	x	x	x	x	x		SPA	127
x		x		x		x		SRA	85
x		x			x	x		SRB	101

1	2	3	4	5	6	7	8		Code
				x	x	x		HLT	112
						x		Modifier, indirect address selection	64

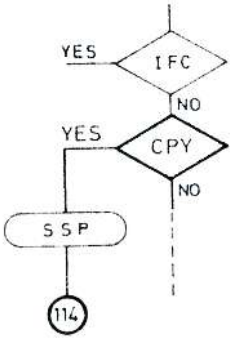
3.3 Core Logic Functions and Operation

In the following logic explanation, references are given to the corresponding pages in Section 9 of the Service Manual. Additional features of the Standard-Logic Model necessitated the following Core Logic changes:

Feature (48-Total Models)	Change in the Core Logic
Indirect address selection for n1	Logic terms added to PC80 and addition of PC72.
Indirect address selection for n2 of CPY	Logic terms added to PC64 and addition of PC75 & PC114.
Indirect address selection for n2 of ADD, SUB, MLT and DIV	Logic terms added to PC82 and addition of PC73.
Feature (12 & 48-Total Models)	**Change in the Core Logic**
Additional PPK Features	Logic terms added to PC89 and PC81.
Improved Punch Buffer Reset	Changed logic terms for PC160
Improved Parity error detection	Changed logic terms for PC52 and PC80
Changed HLT code	Changed logic terms for PC122
SKA and SPA	Logic terms added to PC64.

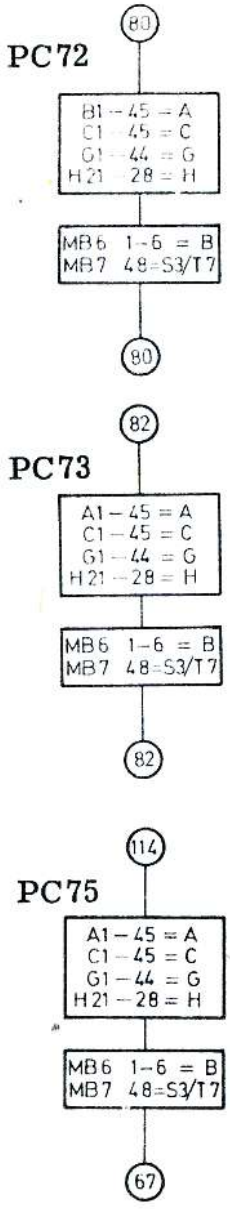
3.3.1 Indirect Address Selection

PC64 (see page 9-192):



If CPY was read, the logic will advance to the new PC114. See PC114.

PC72, PC73 and PC75 - added program counts:



The outputs of Sense Amplifiers MB6 and MB7 are inputs to the Plane Selection Control Circuit, see Fig. 3-6.

MB7 will reset Transfer Circuits T1 thru T9 at P48 time.

This will clear

- in PC72 or PC73: the n1 address which was read in PC0 or PC1;
- in PC75: the n2 address which was read in PC64.

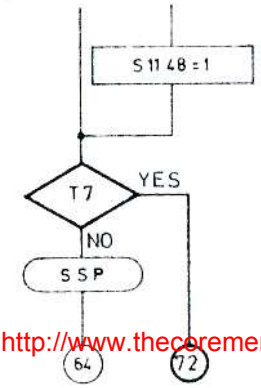
At the following Bit 1 thru 6 times MB6 will set Transfer Circuits T1 thru T6 in accordance with Register B contents.

This completes the indirect selection of the n1 or n2 register.

At Bit 8 time MB6 will set Transfer Circuit T9, Reader ready.

Transfer Circuit T7 will not be set again, so the logic will continue the regular PC sequence when back in PC80 or PC82, as determinated by T7 NO.

PC80 (see page 9-202):

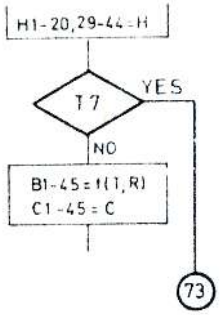


In PC80 the logic tests for selecting the n1 register directly, T7 NO, or indirectly, T7 YES.

For indirect address selection, the logic will go to the new PC72 without completing the SSP.

For direct address selection, the SSP will be completed reading the "f" command.

PC 82 (see page 9-206):

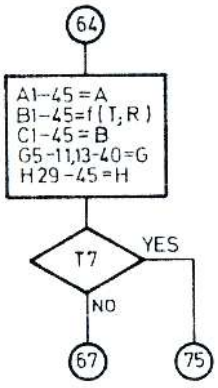


In PC82 the logic tests for selecting the n2 register of ADD, SUB, MLT, and DIV either directly, T7 NO, or indirectly, T7 YES.

For indirect address selection, the logic will go to the new PC73.

For direct address selection the logic will go to PC83 for ADD, SUB & DIV, or to PC25 for MLT.

PC114 - added program count:



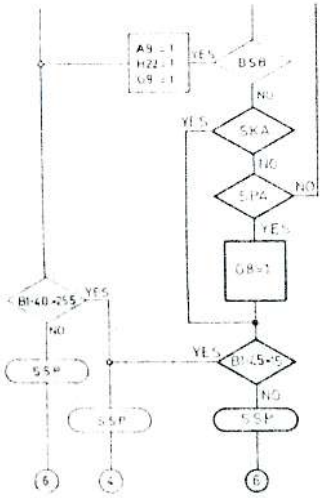
In PC114 the logic tests for selecting the n2 register of CPY either directly, T7 NO, or indirectly, T7 YES.

For indirect address selection, the logic will go to the new PC75.

For direct address selection the logic will go to PC67.

3.3.2 Skip, Reader A or B

PC64 (see page 9-192):



If one of the new commands, SKA or SPA, was read in the preceding PC80, the PC64 logic will select PC6 as the next program count. From PC6 on, the logic sequence for SKA and SPA will be identical to that for BSA and BSB. See page 13-9 in the Service Manual.

To distinguish between SKA and SPA, core G8 will be set for SPA.

The logic will go to PC4 when the contents of the n1 register either exceed 15, are negative, or contain a decimal point. See Item 3.2.3 above.

3.3.3 Additional PPK Features (refer to page 9-211)

The release of the Printer and Data Keyboards and the locking of the Printer Keyboard during PPK does not have to be programmed any more. It is now carried out automatically by the following logic terms which have been added to PC89:

```
S11  = P46
S12  = S11 P46
F1   = S11 S12/ P46
F2   = F7/ P46
F3   = S12/ P46 + F7/ P46
F5   = S12/ P46 + F7/ P46
```

A. Data Keyboard and Function Keyboard Release (DKR, FKR):

In the first PC89 recirculation S12/ P46 will set terms F3, F5, and S11 P46. Then, in PC160, which is a result of F3 and F5 being set, the Output Buffer flip flops FF3 and FF5 will be set resulting in DKR and FKR. See Figure 9-11 in the Service Manual.

B. Printer Keyboard Release (PKR):

During the second PC89 recirculation S11 S12/ P46 will set terms F1 and S12 P46, while S12/ P46 will set F3 and F5. F1, F3, and F5 being set, cause a PKR. See Figure 9-11 in the Service Manual.

C. Printer Keyboard Lock (PKL):

After activating the AB key to terminate PPK, term F7 cannot be set any more (F7 = G/ P21). F7/ will set F2, F3, and F5, resulting in PKL. See Figure 9-11 in the Service Manual.

3.3.4 Improved Punch Buffer Reset (see page 9-229)

The logic equation for Punch Buffer Reset (PB0 = G/ H P46) has been changed.

Term G/ in this equation could result in undesired punching under certain conditions, such as (see page 13-17):

- the Punch Cycle Shaft has turned 180^{o} but SC301 is still closed;
- the logic is recirculating in the PC160 loop which sets core G P46;
- SC107 opens due to an O.L. input.

Since G P46 recirculates during an O. L. input operation (G = G P46), the Punch Buffer cannot be reset immediately upon an SC301 transfer during this time. Punch Clutch Solenoid L309 will thus remain energized longer than necessary which may result in an undesired repeated punch operation.

To overcome this condition, term G/ has been replaced by S10/: PB0 = S10/ H P46. Core S10 P46 can be set only in PC160 of a punch operation:

S10 = F2 F6 G/ H S5 T9 P46
F2 = Punch operation (OFS1-4, OFP1-2, ORA1-2, ORB1-2, PPK)
F6 = no Parity Check Failure
G/ = logic recirculating in PC160
H = Punch Buffer not set
S5 = Punch Cycle Shaft between 270^{o} and 60^{o}
T9 = Tape Reader ready

3. 3. 5 Improved Parity Error Detection

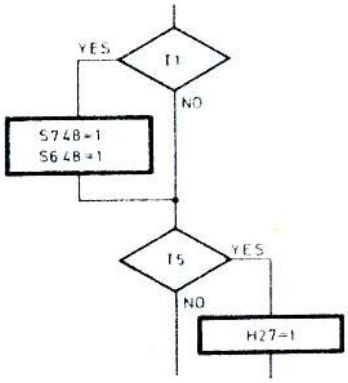
When an n1 address including a hole in channel 1 or 5 is read in during a punch operation the present logic design may result in a false Parity Check.

Example No. 1	Example No. 2
Program:	
0 OFP2 C END 16 OFP2	0 OFP2 C END S1 .....
Logic Sequence:	
PC80: H = T5 P28	PC80: S5 = T1 P48
Misc. Logic: G = G/ H SC304 P28 MB5 = G P28 Parity FF = MB5	Misc. Logic: H = S5 SC304 P48 MB5 = H P48 Parity FF = MB5
PC160: F6 = F6 G/ P28	PC160: F6 = H/ S3/ P48

When the n1 address is read in. Switch SC304 can still be set according to the Even Parity Code for character "C" causing the setting of the G P28 or H P48 core. This will prevent the logic from leaving PC160 since F6 cannot be set any more.

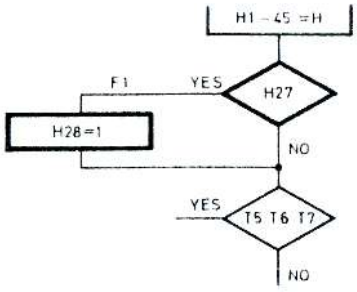
Logic Changes to overcome this possible malfunction:

PC80 (see page 9-202):



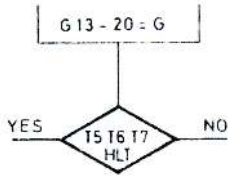
The time between the preceding punch operation and the setting of cores H P28 and S5 P48 has been increased: with T1YES, core S7 P48 will be set during PC80. In PC64, after the additional time delay due to the SSP in PC80, core S5 P48 will be set by S7 P48.

PC52 (see page 9-186):



With T5YES, core H P27 will be set during PC80. In PC52, after the additional time delay due to the two SSP's in PC80 and PC64, core H P28 will be set.

3.3.6 Changed HLT Code



The PC122-logic will recognize only T5T6T7 as HLT.

See page 9-214 in the Service Manual.