Content-Addressable and Associative Memory Systems

A SURVEY

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Abstract—**This review of content-addressable memory and associative computer systems represents an attempt to consolidate and report nontechnically the direction in which numerous independent research programs have progressed during the last ten years. The paper reflects the views of a myriad of researchers on subjects of organization (configuration concepts), hardware elements, logical operations, speed, cost, size, software implications, applications, advantages and disadvantages. In a report of this type it is important to quote directly and indirectly from the researchers themselves, so that the trends or directions of their concepts may converge into meaningful information. Acknowledgement is made to those quoted (see bibliography references) since they represent the meat of this survey. The bibliography, although voluminous, is not necessarily complete. A number of reference sources may have been overlooked inadvertently. It is hoped, however, that the information and the bibliography will serve as a base for those entering into research connected with this rapidly developing concept.**

I. Introduction

ASSOCIATIVE memories have been generally described as a collection or assemblage of elements having data storage capabilities, and which are accessed simultaneously and in parallel on the basis of data content rather than by specific address or location.

A memory, which in one word time finds a matching segment and reads the remainder of the word, has been called by one of these names: Catalog Memory, Associative Memory, Content-Addressed Memory (CAM), and Data Addressed Memory (DAM). As yet, there has been no one standard name designated [2].

The adjective "associative," when applied to memories or computers, was probably derived from theories concerning operations of the cells of the brain. The term is more applicable to the function of recall by association of ideas. Correctly, when applied to computer hardware, the meaning of "associative" refers specifically to interrelationships between data, and not to the storage mechanism. Storage mechanisms are organized specifically to assist in performing the functions of data association. It seems more appropriate to call storage elements organized in this fashion content-addressable memories (CAM).

Manuscript received May 2, 1966.
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A. Purpose of This Study

The primary purpose of this study is to provide information bases on which recommendations can be made concerning future efforts in this area. A survey of the literature in the field, as indicated by the voluminous bibliography, provided useful data on hardware, software, applications, and concepts which are to some extent summarized in the following pages. Direct and indirect quotations of the authors are used liberally in order to preserve accuracy in the reporting. Comprehensive technical investigations of the processing elements used are left to the resources of the research laboratory.

II. Configuration Concepts

Three concepts are emerging from current work in the field:

1) a content-addressable memory, which is used as an extension of a conventionally organized memory, for the performance of a variety of logical search and match operations;
2) a content-addressable memory, large enough to act as a special purpose primary data storage and retrieval device; and,
3) an "associative" processor, containing a content-addressable memory with cells capable of arithmetic and associative logic in addition to the search and decision logic.

In all these arrangements, the memories are "word-organized" for reading and writing operations. However, they may differ in their logical organization in that they are fixed or variable. In the former case, a fixed portion of the word is set aside for interrogation and all of that portion must be used for an interrogation. A variation of this divides the word into fixed segments, any of which can be used as the interrogated portion. All the bits in the interrogated segment must be used in the interrogation. The variable type may have a fixed segment, but any part of this segment may be interrogated. The fully interrogable memory allows any choice of bits in the word to be used in the interrogation, and the remainder of the word to be read. This is the most general form of the content-addressable memory [1]. It

is common practice to divide the "word" into tag and data portions in order that those words meeting the search criteria may be marked for subsequent operations.

A. Auxiliary CAM

Content-addressable memories have been proposed as adjuncts to conventional systems. Davies [18] suggests that a set of keys can be stored in a small associative memory. Records stored in main memory can be checked serially but simultaneously against a number of keys for match. Fuller [30] investigated the utility of content-addressable memories (CAM's) within a general purpose computing system. In the process of working toward this objective, the CAM organization was constrained to remain a special purpose memory and was not given the extra hardware required to do more powerful external arithmetic and logical operations. It is assumed that CAM exists as a subsystem for a controlling computer which can present instructions and key words to CAM, call for data transfers between its internal memory and CAM, and execute various tests of CAM. In this context the controlling computer provides hierarchies of conventional memory, high speed arithmetic and logical capability, and flexible input-output facilities, making use of the CAM system in an associative mode only where it provides advantages over conventional facilities.

Ewing and Davies [24] considered two approaches in their design of an associative system, one of which added an associative memory to a more or less conventional computer. The alternative approach involved a new organization, developed around the principle of memory distributed logic. The former approach provides a random access memory for program storage and a bit serial associative memory for data storage and parallel processing. In the organization considered, the random access memory contained 4000 twenty-four bit words, and the associative memory contained 500 ninety-six bit words.

Kaplan [54] presents a system design for a search memory subsystem to a general-purpose computer. The structure postulated consists of a main computer memory which communicates via a memory register with the search memory subsystem.

Nissim [85] is a proponent of content-addressable "scratchpad" memories used in conjunction with larger slower memories of the conventional type. In this way, he suggests, there is an apparent overall increase in memory effectiveness.

It is clear that much interest has been generated toward the minimization or total elimination of many of the burdensome bookkeeping operations connected with the use of conventionally organized memories. A major share of computer software effort is involved with these housekeeping routines. Content-addressability of memories would tend to ease the tasks of the programmer in this respect.

It is conceivable that the minimization and elimination of progam housekeeping routines could significantly reduce operating time, particularly where the routines are required to be called in from the slower operating input-output devices. The reduction of operating time and the saving of software effort would appear to more than justify the extra cost required to logically connect the auxiliary CAM to the conventional system.

B. CAM as Primary Storage

Except for "associative processors," which are discussed in Section II-C, much of the effort in designing content-addressable memories has been directed toward special purpose applications. Foremost among these is information retrieval, which for the most part does not require arithmetic operations other than counting. These special memories are used mainly for retrieval of filed information by means of matching operations using such criteria as Equal To, Greater Than, Greater Than Or Equal To, Between Specified Limits, Next Highest, Next Lowest, Highest In Memory, Lowest In Memory, and their inverses.

Ahrons [1], [2], Barnard, et al. [6], Falkoff [25], Kiseda, et al. [37], Lee [62], [63], McDermid and Petersen [75], and others concentrated on designing memories from particular elements to accomplish the logical operations stated above. Their efforts were more in determining the feasibility of operation of content-addressable memories for the special purpose, rather than the general purpose application.

C. The Associative Processor

There is a natural dissatisfaction inherent with computers that are limited by special purpose applications. Consequently there is a normal evolutionary trend to establish general purpose designs. A number of designers are contemplating content-addressable memories which are fully associative (i.e., each cell is "associated" with its neighboring cells) and also capable of performing arithmetic operations. Notable among these are the Solomon Computer (Slotnick, et al.) [115], the Orthogonal Computer (Shooman) [30], the Spatial Computer (Unger) [119], [120], the Pattern Recognition Computer (McCormick, et al.) [30], and the Holland Machine (Holland) [44], [45]. These cellular or distributed logic computers [30] are capable of handling the usual arithmetic operations, Logical AND, Logical OR, Shift, Expand, and others. Fuller [30] concludes that cellular or distributed logic computers have not gained significant acceptance to date for at least two reasons. The cost of such structures is high and their recognized range of application is small.

III. Hardware Elements

Early work in content-addressable memories was accelerated by cryogenic or superconductive developments. As early as 1956, Slade and McMahon [110] published a paper describing a catalog memory using cryotron elements. This work was expanded by Slade and Smallman in subsequent reports [111]–[114]. Crowe [17] built and tested a memory cell based on trapped flux in superconductors and reported the results in 1957. The development stages behind the effective application of the superconductive phenomenon are traced by Ahrons and Burns [2] in their review of superconductive memories.

Although it has been generally conceded that cryogenic elements could be economically mass produced, it is also agreed that the cost of refrigeration needed is prohibitive. In addition, the problems associated with maintenance of refrigerated elements caused some apprehension.

Partially because of these reasons, others began to direct their efforts toward the use of noncryogenic components. This latter effort appears to be rapidly pyramiding due to recent developments in thin films and integrated circuits. The construction of content-addressable cells from combinations of these new elements appears more economically feasible than those with cryogenic elements.

Ittner [50] argues that it has not been possible to show that cryogenic circuits possess, on balance, any functional advantages over circuits realizable in competitive technologies. The cryotronic technology, while possessing a number of special features, is functionally equivalent to a number of existing technologies and must, therefore, be evaluated basically in terms of the function it can provide for a given cost.

Maguire [71], in his review of work on superconductive memories in late 1961 stated that the following expectations were shown:

a) all-superconductive computers will emerge from the laboratory into the marketplace within 10 years;
b) high-capacity thin-film cryotron memories will provide the engineering wedge, but a minimum of 10^5 to 10^7 elements must be successfully assembled to justify the refrigeration cost;
c) superconductivity, "the ideal computing technique," is still in the research stage, but it may forge ahead of competing high-capacity, high-speed approaches in the long haul because the difficulties of batch fabrication have been met head-on from the beginning.

Although work continues in the cryogenic medium an increasing awareness is becoming evident that noncryogenic devices may provide the means for advancing the state-of-the-art of content-addressable memories at an increasingly greater rate.

Other elements being investigated for content-addressable memories are variously described as:

Tunnel Diodes [30], [85]
Evaporated Organic Diode Arrays [68]
Magnetic Cores [30], [49], [57], [75], [125]
Plated Wire [24], [30]
Thin Permalloy Film on Copper Wire [30]
Semiconductors [65]
Transfluxors [70]
Biax Cores [73]
Laminated Ferrites [124]
Magnetic Films [95]
Solenoid Arrays [88]
BICORE Thin Film Sandwiches [30]
Multi-Aperture Logic Elements [118].

Fuller [30] discusses in detail CAM systems using tunnel diodes, ferrite ring cores, thin Permalloy films, and crossed-film cryotrons. Critical properties considered in systems constructed from these elements are:

a) energy required to set an element
b) energy which may be extracted from an element by nondestructive readout (NDRO)
c) ratio of NDRO signal for a stored "1" to NDRO signal for a stored "0" (signal-to-noise ratio)
d) switching time of a memory element
e) transmission characteristics for drive and sense lines which link many memory elements.

The first two properties determine the gain required of peripheral circuitry, hence its speed and complexity. The SNR determines the number of bits in each word which may be interrogated simultaneously. All properties influence execution time for commands.

IV. Logical Operations

A. Memory Element Operation

The basic storage element of the content-addressable memory has the property that it may be read into, written into and compared with external information. In the majority of designs it also has a characteristic of being organized with other memory elements, such that matching operations are carried on in a bit-serial word-parallel fashion. That is, the first bit of each word is looked at simultaneously for match, then the second bit, etc., until the entire memory is scanned. If only an exact match is desired, the operation can be entirely parallel and simultaneous for all bits of all words. However, in order to introduce sorting techniques, it is desirable to scan bit by bit from the high order bit position of each word to determine the proper sequence of reading out of data.

Most designs utilize a two component per bit type of

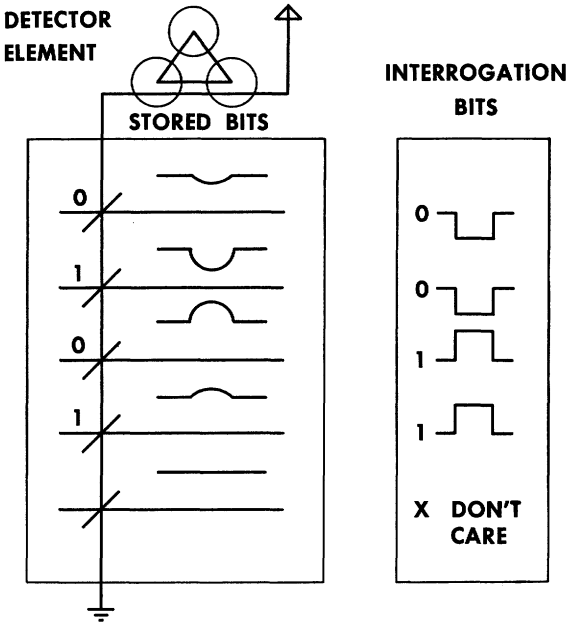
operation in order to locate data stored anywhere in a content-addressable memory. There must be a means for performing a nondestructive comparison of the associative criterion with every word in memory; this must be coupled with a means for identifying a matching word; and finally, there must be a means of access to the matching word location to provide a subsequent readout [57]. Normally, the associative criterion consists of the data portion and the mask portion. The data portion is the known segment of the word being looked for. The mask portion represents those bit positions in the word which should be ignored during the search.

The logic performed at the cell is both binary and ternary, such that comparison can be carried on in addition to storage. The interrogate signal has three states: 1, 0, ϕ (don't care). This latter signal is utilized for performing the masking operation.

McDermid and Petersen [75] clearly illustrate the memory cell operation, as shown in Fig. 1.

Thus, for conditions of mismatch between stored and interrogating information a large signal is generated. The role of the detector is to register only the first large signal regardless of polarity and to be insensitive to the small output signals. In this system interrogation is done parallel by word, serial by bit; i.e., the bit planes are pulsed in time sequence.

The usual technique for achieving the required outputs is to use a pair of elements or even two pairs to provide unipolar mismatch and nulled-match outputs. Aside from requiring extra elements, these techniques inevitably depend upon the ability to cancel outputs from many pairs and, therefore, require very strict control of film output uniformity [95].



Stored Signal	Interrogation Signal	Output Signal
0	0	small negative
1	0	large negative
1	1	small positive
0	1	large positive

Fig. 1.

The store is thus organized in two parts, one containing information in true form, the other in complement form. The search register which holds the key for the search controls the bit drivers. A "0" in the search register drives the true side of the memory, a "1" drives the complement side.

The output of the cryotron catalog memory of Slade and Smallman [114] is a yes or no answer as to the comparison. All bits of the memory are interrogated in parallel with either a positive or negative current and these interrogate currents either add to or subtract from the persistent current in the memory cells. When the interrogate current and the persistent current are additive, their combined magnetic field is sufficient to cause the corresponding gate in the gate network to become resistive. If the interrogate currents match all of the persistent currents for one word of the memory, then all of the gates in that word become resistive and a voltage will appear at the memory output terminals. Unless there is an exact comparison there will always be at least one superconducting path through the memory and there will be no voltage output.

B. Compare Operations

The following comparison operations have been considered for content-addressable memories:

Equal	Not Equal
Less Than	Greater Than
Less Than Or Equal	Greater Than Or Equal
Maximum Value	Minimum Value
Between Limits	Not Between Limits
Next Higher	Next Lower
Similarity	

By use of the masking technique, the similarity operation is used to search for words which have some part, but not all parts in common with each other.

C. Input-Output

The possibility of occurrence of multiple responses to a search makes it necessary to provide some method of tagging words for subsequent retrieval. Storing of data also requires some means of finding "empty" locations or "available" memory cells.

Tagging implies additional operations such as tag writing, tag clearing, tag complementing, and tag copying. The search operation is relatively basic; what to do with the data when it is found may add considerably to the complexity of the design.

V. Speed, Cost, and Size

A. Speed

On the average, a search for a word in a random access memory would consume the time required to scan and compare one-half the memory. As memories become larger, this time requirement becomes excessive and, therefore, this scanning procedure has limited use [2]. In operations such as file searching and correlation, if n words are stored and n correlations are needed, the execution time with conventional sequential processing is proportional to n^2; in content-addressable systems, execution time is proportional to n [16].

It is widely felt that further increases in computation speeds of digital computers are more likely to occur as a result of changes in computer organization rather than component and circuit improvements, as has largely occurred in the past [30]. The speed of the associative memory is independent of the number of words, whereas the speed of the random-access memory is proportional to $n^{1/2} \log_2 n$ [1]. With sequential logic and the high degree of parallelism coupled with the fact that a minimum of transfers will be necessary, it may be possible to build an ultrafast system at a reasonable cost [9].

Information may be retrieved at a rate which is largely independent of the amount of information present in the memory [63]. Lewin's series-parallel readout method (with two sense outputs for each digit of the word) requires only $2w-1$ cycles for complete readout of w words with the same initial interrogation segment [67]. Lewin's method may be modified to one sense output per digit if the sense can determine a match either between 1's or 0's. This method requires $2(2w-1)$ cycles [1]. Miller [77] describes an interrogation routine which retrieves k multiple responses in, at best, $(k+1)$ memory cycles, and, at worst, $(2k-1)$ memory cycles. This compares with Lewin's method which always requires $(2k-1)$ memory cycles.

In 1956, it was calculated that a cryotron memory could be interrogated every 10 microseconds and a new word written in about 500 microseconds [110]. In Davies [18] superconductive memory organization, the speed of the cross-film cryotron circuit is intimately associated with the gain of the cryotron (approximately 300 nanoseconds for the configuration and parameters given in his example). Newhouse, et al. [81], estimates the feasibility of a 300 000 bit memory with a 50 microsecond comparison cycle time.

In 1961, Maguire [71] reported that a bit organized memory driven by cryotrons and designed for speed was in the research stage at IBM. Using alloy film gates, with an insulation thickness of 5000 A, calculations indicated a loop time of 1 nanosecond, thereby projecting a memory cycle time of 10–20 nanoseconds.

Command execution times for various memories constructed of tunnel diodes, ferrite ring cores, thin Permalloy film plated on copper wire, and cryotrons, range from 70 to over 700 nanoseconds for various operations. The cryogenic memory is indicated as the fastest for searching, but slightly slower for other operations than the memory constructed with thin Permalloy film elements [23], [30]. For most operations the thin Permalloy film content-addressable memory appears to be fastest [22].

Comparison of microferrites and thin films shows that in the near future both approaches are likely to provide 100 nanosecond memories of several thousand words [94]. An evaluation of various core materials in the elastic switching mode indicated a maximum speed of 100 nanoseconds per operation [49]. There is a notable increase in speed reported in a relatively short period of time. In 1961, search and retrieval times for an n-word associative memory described by McDermid, et al. [75], requiring a search on 36 bits, would be approximately 6 microseconds. Lussier, et al. [70] describe an application of all-magnetic logic in a design of a content-addressable memory with a total retrieval time of 10 microseconds, using commercially available ferrites.

UNIVAC has a thin-film 300 nanosecond search memory constructed with BICORE elements. Basic switching time of the BICORE is said to be about 6 nanoseconds. Access time for all bits ranges down to 100 nanoseconds. The memory is considered to have the potential to do a complete search in 100 nanoseconds; that is, it could compare one million incoming data words with all the stored key words in 0.1 second [15], [124].

Kaplan [54] postulated a structure with a search memory subsystem that executed a 36-bit equality search in 8.0 microseconds. A very complex six-field, six-bits-per-field quantitative search required 16.0 microseconds and an average search 12.0 microseconds. The time required to execute a search is a function of the number of bits searched, the mode of search, and the number of fields. Total search time is 0.1 microsecond per bit for equality, greater than or less than, plus 1.1 microseconds per bit searched for next higher or next lower, plus 1.0 microsecond per field searched (except first field), plus 4.0 microseconds to get to the next instruction. (Operation times were quoted for UNIVAC BICORE elements.)

A transfluxor memory achieved cycle times of 3.0 microseconds for write and 10 microseconds for interrogate and readout [96]. The Goodyear MALE (multiaperture logic element) memory required 2.5 microseconds for the read and compare operation and 5.0 microseconds for the write operation [118]. Nissim [85] states that tunnel diodes appear to offer the best practical approach to random-access scratchpad memories, with cycle times in the 10–100 nanosecond range. A 16 384 20-bit word solenoid array memory described by

Pick [88] has an access time of 0.7 microsecond and its cycle is below 2 microseconds. This memory utilizes an associative technique to allow addressing of any of its 1024 sixteen word data-containing sheets.

A few words should be said relative to the fully associative processors. The SOLOMON Computer [115] indicates a speed gain of from 60–200 over large scale conventional computers, depending on the amount of parallelism inherent in the problem. A speed gain of 33–660 relative to conventional computers with equivalent memory cycle times is reported for the Orthogonal Computer [30]. Barnard, et al. [6] reports the following cycle times (in microseconds) for operation of a cryogenic associative processor with 5000 72-bit words:

Write	3.0
Compare and Read 1st Word[1]	$6.0+k$
Consecutive Read	$0.85+k$
Compare	2.5
Selective write (after tagging)	3.2
Greater Than { Average[2]	$1.4B$+Read
Less Than { Worst	$2.8B$+Read
Between Limits Average	$2.8B$+Read
Between Limits Worst	$5.6B$+Read
Next Higher (Lower) Average	$5.0+2k$+Read
Next Higher (Lower) Worst	$(7.0+k)B$+Read

Feldman [26] discusses an efficient way of simulating an associative processor on conventional computers. (The TX-2 at the M.I.T. Lincoln Laboratory was used as the vehicle for the simulator.) He states that the times of the simulator are sufficiently small to raise questions about competing with hardware techniques, and that it should be feasible to build a system which loses a factor of about two in storage and three-to-five in time against an associative memory of the same basic speed. The implication here is that it is debatable whether it will pay to build hardware associative memories for general purpose use.

At any rate, for problems allowing unordered data sets, the content-addressable memory achieves the advantages of list storage with a significant speed gain.

In summary, with respect to speed, two approaches are at the forefront; microferrites of a drastically reduced element size, and thin magnetic films deposited by vacuum evaporation or electrodeposition. According to recent publications they are comparable in speed attained to date. It also appears that the use of noncryogenic elements will eliminate the necessity for costly refrigeration systems.

B. Cost

The major drawback to development of content-addressable memories is the lack of a suitable associative cell in a practical technology at an acceptable price. Interest in this type of organization has been heightened by recent advances in batch fabrication techniques involving deposition and etching of metallic semiconducting, insulating, and magnetic thin films to form intricate multilayered patterns. It is hoped that these techniques will allow economic fabrication of a complex network of identical molecules [30].

Feldman [26] implies that software associative processing is much cheaper than specially built hardware, is more flexible, and is virtually unlimited in size. However, Prywes et al. [93] consider the content-addressable memory a necessity for multilist processing techniques.

Speed is inherently expensive. Cells constructed in a model described by Lee [66] cost $3.80 for total components. Logically equivalent, but slower circuits with large matrices (at 300 kc/s rates) could be constructed at $1.55. The future cost picture looks promising. High-capacity thin-film cryotron memories may provide the engineering wedge, but a minimum of 10^5 to 10^7 elements must be successfully assembled to justify the refrigeration cost [71]. Magnetic random-access memories have the cost advantage for small capacities and superconductive memories appear to have the cost advantage for very large capacities. The crossover point has been estimated in the 10^6 bit magnitude. This estimate includes refrigeration [2].

An associative system where the memory, arithmetic, program, and instruction decoding and modification functions are all contained within the main store, may be highly economical because of the mass-fabrication of cryotrons. Hundreds or thousands of active devices are made at once, together with their interconnections on a single substrate [9].

The SOLOMON Computer with 1024 elements is estimated at $5 000 000 [3]. The Holland Machine should be significantly more expensive, because of more complex local control, for an equivalent number of processing elements [44], [45].

The solenoid array described by Pick [88] has a bit cost ranging from a half a cent per bit for large memories to a few cents per bit for relatively small ones. Nissim [85] compares (in 1963) the cost of tunnel diode vs. core associative memories:

Size	*Speed*	*Cost*
Megabit (tunnel diode)	10 nanosecond	$5–10/bit
Megabit (core)	1–5 microsecond	10–25¢/bit

Although the sources quoted appear to give greater weighting to the potential of the cryogenic mass memory, the promises of low cost noncryogenic elements should not be discounted, especially considering the improvements in fabrication and the current rate of invention.

C. Size

It is difficult to divorce the size of a memory from the cost of the elements used in the assembly. An equally important aspect, however, is the limitation imposed

[1] k = Switching time of small ladder estimated at 4–5 microseconds.
[2] B = Number of bits in field of interest.

technically. One of the most important limitations to the size of a memory is the half-select noise which appears in the sense. If this half-select noise is dependent on the "1" or "0" stored information in the half-selected cells, it cannot be eliminated by balancing techniques and thus with greater memory size eventually half-selects overcome the possibility of detecting a sense signal [2].

The word capacity of associative memories is restricted primarily by the interrogation drive problems. It is reasonable to conclude that with optimization of components and distributed drive techniques, larger associative memories (for example, 4000 words×72 bits), operating at a 10 Mc/s search rate can be developed [57]. Results of research by McDermid, et al. [75] indicate that word lengths up to 36 bits with a passive detector are feasible; however, word lengths of 1000 bits are technically achievable with an active element as the detector. Memory capacities of several hundred words appear technically feasible with a single interrogation driver; for larger sizes, parallel operation may be required. Hunt et al. [49] estimated in 1964 that a memory of 1000 words with lengths up to 100 bits would be achievable with a single set of peripheral circuitry.

Bit densities of 1000 bits per square inch have been successfully operated. The superconductive memory appears attractive not only for random access memories, but also for associative memories [2]. A gradual increase in storage capacity, beyond today's few million bits, may result from batch fabrication of magnetics, but a significant increase requires methods of batch fabricating both the magnetic and the associated semiconductor devices. Capacities of hundred millions or billions of bits are likely to be attained sooner by superconductive techniques [94].

It is estimated that high speed associative memories commence being generally attractive at about 10^7–10^8 bits. Presently most advanced random-access memories are in the 10^6–10^7 bit range [1]. Rajchman's memory survey, in 1963 [94], indicated that the largest memory in use has a capacity of two million bits, and the fastest a cycle time of 375 nanoseconds.

RCA's superconductive continuous sheet memory appears to show promise for large capacity random-access memories in the 10^7 or near 10^7-bit range . . . and potential for the 10^9 bit size. Further in the future is the possibility of developing the "long-sought-after" content-address memory large capacities [2].

A 360 000 bit solenoid memory has been built with about 100 planes. The signal degradation in increasing the number of planes from a few to a hundred was minor [88]. The performance of small transfluxor arrays indicates that capacities of 2000 words and 48 bits are feasible. The number of words is limited by the maximum back voltage during interrogation (70 volts for 2000 words); the number of bits is limited by the signal-to-noise ratio and is dependent on the means used for match detection [96].

The numbers of elements used in connection with providing the logic for the content-addressable memory cells is high. The IBM research 256-bit cryotron memory requires 2435 cryotrons plus 1118 for reset, or 3553 in all [71]. Unger's SPAC (*SPA*tial *C*omputer) [119], [120] was a simulated array of 36×36 modules. A module consists of some logical circuitry, a 1-bit principal register, and a set of nine 1-bit memory registers. Each module required 170 gate inputs including link circuitry. The Pattern Recognition Computer [30] consisted of 1024 stalactites (elements). The hardware per stalactite was 49 transistors, 230 diodes, 54 capacitors, and 248 resistors. The Holland Machine [44], [45] had $n+14$ memory elements for each word length "n" for each processing module. Several hundred gate inputs would be required for each module. The SOLOMON Computer [115] postulated a 32×32 matrix of processing elements (1024 cells). Processing element hardware is estimated at 6 memory elements, 200 gate inputs, 2 write, and 2 sense amplifiers.

The MIRF (*M*ultiple *I*nstantaneous *R*esponse *F*ile) system designed for Rome Air Development Center has a design capacity of 3000 words. About 300 current drive transistors, 2500 logic transistors, 2500 printed gates (6 resistors, 2 capacitors, and interconnecting wiring on a passive substrate), and 5000 diodes are used in the system.

Auxiliary subsystems include a 500 96-bit word memory considered by Ewing and Davies [24] as auxiliary to a 4000 24-bit word random access memory, and Kaplan's search memory [54] containing 4096 words of 72 bits each. In the latter, searches were carried out on 36 bits, with the remaining 36 bits entered into the accumulator on a match condition.

VI. Software Implications

The existing literature on programming an associative processor is mainly concerned with special applications and is at the machine language level.

Two observations may be made in regard to random-access memories.

a) A large percentage of programming time and effort is usually spent in assigning and keeping track of addresses, and
b) in so far as is known, the human memory allows information to be retrieved by an associative process without regard to physical location of information.

Thus, the conventional technique of requiring an address for each physical word location may be neither the most natural nor the most convenient [1].

The notion of addressing by contents enables us to avoid the artificialities of location assignments and frees us to a large extent from such local considerations

as scanning, searching and counting [63]. The ability to address data in a content-addressable memory by cell content rather than cell location suggests its use in problems for which list-organized memories have been found convenient. These problems include game playing, theorem proving, compiling, scheduling, and real time control. List organized memories, like content-addressable memories, allow dynamic storage allocation, but differ from content-addressable memories in that data within a list structure is inherently ordered with defined predecessors and successors, where data sets within content-addressable memories are unordered [23].

Location addressing becomes cumbersome and content addressing efficient when

a) data is to be addressed by several sets of reference properties;
b) data elements are sparse relative to values of the reference property. Location addressing is often forced to assign cells for which no data is stored;
c) data become dynamically disordered in memory during processing [30].

In a content-addressable memory, the key may be the stored word or pattern or any number of bits selected from any portion of the stored word. It allows data stored to be located and retrieved though their physical addresses are unknown, and without recourse to sequential search. On recognition of a key, either the whole word or any part of it or its address may be retrieved nondestructively. Only one cycle time is needed to determine if a desired word is in storage, and another cycle to retrieve it [16].

The associative processor suggested by Barnard, et al. [6] features sorting, selective writing, marking, next higher, next lower, and range retrieving. Such operations in a conventional random-access memory would require complex housekeeping programs for accessing and comparing the contents of each cell of memory with the contents of all other cells. The selective write feature of the associative memory has the capability of inhibiting selected bit positions from a writing operation and the ability to write into more than one word simultaneously. Time saving is inherent in such operations, where a minimum of internal transfers will be necessary.

In a sense the associative processor can be microprogrammed. The concepts inherent in the associative memory have been extended in the associative computer to perform general computation simultaneously throughout an extended periodic structure. Such an organization is particularly suited to the type of computation in which the same program must be performed on a large number of data sets. This is characteristic of many data processing problems and of a number of scientific calculations as well [19].

The method by which associative instructions are controlled constitutes one of the major factors contributing to the flexibility of the associative processor. Each field of the instruction directly specifies some control function, so that numerous associative instructions can be microprogrammed by the appropriate selection of fields [24].

Instructions for content-addressable systems may look quite different from those used in conventional systems. Various tagging operations may be accomplished by varying bits in a single TAG instruction, which essentially acts like a macro order. The instruction "RETRIEVE" is a similar example resembling a macro instruction.

The number of functions which an associative memory can perform may be broadly classified in the following ways.

a) Search Functions (exact match search; limit-type searches, including greater than, greater than or equal to, less than, and less than or equal to); pattern recognition; supplementary search operations including ordered retrieval, minimum and maximum searches, nearest neighbor, and composite searches.
b) Writing Functions including sequential load, random load, load first empty location, write "don't care" bit, field alteration, and memory partitioning.
c) Associative Memory Readout Function such as address readout, data readout, multiple match resolution, yes-no decision operations, and count of matches [73].

Prywes, et al. [93] and Rosin [98] suggest that programs can be retrieved by name rather than by location, thus allowing for a greater vocabulary and ease of communication with the computer. The associative property of the memory allows the machine to be used so that symbolic names in source language programs need not be translated into numeric addresses. Table entries are determined by order and relative to a tag, thus these need not be contiguous. This diminishes the storage allocation problem to a very great degree. Moreover, the corresponding pass in an assembler or compiler is not needed, resulting in a real saving of computer time.

VII. Applications

Suggested applications for which content-addressable memories and associative computers appear to be ideally suited are legion. They range from commercial to military to scientific and may be broadly segregated into file processing or computational tasks. For the purposes of assembling the numerous applications into some reasonable order, they are grouped below in categories of File Maintenance, Pattern Recognition, Mathematical, Information Storage and Retrieval, Translation, Military, Communication and Transportation, and Miscellaneous. As is usually the case, some applications may overlap into other categories. For the purpose of

simplicity, the applications are assigned only to one category.

A. File Maintenance

Those applications suggested for updating and processing of existing files are:

Sorting, merging, ordering, collating
Inventory control
Payroll
Computer software storage
Table look-up
Telephone service look-up
Personnel file maintenance
Department store customers' files
Automatic mail sorting
Toll ticket reading
Scheduling
Compiling.

B. Pattern Recognition

Those applications suggested that are akin to machine recognition techniques are:

Pattern recognition for molecular and biological structure analysis
Photographic analysis
Character recognition.

C. Mathematical System Solution

Applications suggested in connection with scientific calculation are:

Game playing
Theorem proving
Function optimization
Solution of elliptic partial differential equations
Determination of critical paths through a graph
Interpolation
Solution of linear equations
Calculations of inverses and eigenvalues of matrices
Correlation and autocorrelation
Numerical solution of systems of ordinary and partial differential equations
Orbital track calculation
Hydrodynamics
Heat flow
Diffusion.

D. Information Storage and Retrieval

Of all the applications suggested, the foremost is concerned with some phase of information storage and retrieval. This includes the following functions:

Data retrieval, including cross retrieval, erasing, gap closing and preference
Cataloging
Library and catalog search files
Document retrieval
Technical information file maintenance.

E. Translation

The characteristics of content-addressable memories make them ideally suited for conversion of data from one form to another in tasks such as:

Language translation
Code conversion
Translation of mnemonic operation codes to machine codes in program assembly operations.

F. Military

A number of military-oriented applications are suggested as likely candidates in the use of content-addressable systems:

Radar-track correlation
Processing sonar returns
Military intelligence analysis
Real-time vehicle surveillance (satellites)
Undersea target identification
Photoreconnaisance
Command and control
Armament deployment
Tactical battle condition determination
Symptom-cure checkout of orbital systems
Guidance and control
Radar-data processing.

G. Communication and Transportation

Air traffic control
Real-time control.

F. Miscellaneous

A number of special purpose and miscellaneous applications are suggested as follows:

Numerical weather forecasting
Nuclear reactor calculations
Nuclear particle track analysis
Data correlation
Statistical data analysis
Real time applications
Artificial intelligence
Parallel processing
Data reduction
Medical diagnostic tables.

All of the applications listed above above were suggested by those persons actively engaged in either theoretical or actual research in the area of content-addressable or associative systems. Except in the case of information storage and retrieval and some algorithms formulated for solution of some mathematical systems, the superiority of the content-addressable memory or associative processor is only implied, not proved. There is, however, sufficient reason to believe that enough applications can be found to justify such organizations, even if only as auxiliary hardware to conventional systems.

VIII. Advantages and Disadvantages

A. Advantages

The major advantages that content-addressable systems appear to offer are in speed and particular cell organization which lends itself to batch fabrication of fault tolerant structures.

The recognition technique permits the content-addressable memory to compare the data in search registers with every word stored in one memory cycle. It does the equivalent of the many thousands of load and compare operations that would be required with a conventional organization in such operations as sorting, file searching, and correlation [16].

Considerable processing time is saved because:

a) it is not necessary to store data in sorted order;
b) lookups can be made on the basis of different keys at different times over the same data;
c) records need to be stored only once;
d) addresses are not needed to store records [18].

Organization of random access memory into list structures slows problem execution due to time spent in forming lists, searching lists, retrieval of data at large known depth within a list, erasure of lists, and transfer of lists to and from bulk storage. For problems allowing unordered data sets the content-addressable memory achieves the advantages of list storage with significant speed gain [23].

In addition to parallel computing capability, other advantages of the content-addressable system are as follows.

a) Data storage and retrieval capabilities which greatly simplify or eliminate such common data manipulations as sorting, collating, searching, matching, cross referencing, updating, and list processing.
b) Programming simplifications based upon the possibility of ignoring the placement of data in memory and the extensive use of content addressing and ordered retrieval.
c) Periodicity of structure lends itself to integrated circuit techniques and batch fabrication. Interconnections between components become shorter and less tangled, reducing propagation delays and simplifying layout and checkout. Since the structure is periodic, it can be easily expanded in size.
d) The periodic structure may permit an organization which is tolerant of memory or circuit element failures. If a cell fails, it may be possible to avoid its further use with little loss to the system capability. A program for an associative structure makes little or no reference to a unique cell so that loss of a cell would not confuse the program [24].

The complexity in the memory logic diminishes the need for some of the complexity in the control circuits, hence, fewer different masks are needed when preparing circuitry. The ability to disable a cell by tagging it with a disable bit scheme decreases the problem of maintainability [98].

Numerous statements have been made as to the advantages of the cryotron as a device to be used for content-addressable and associative systems. A major advantage of cryotron elements is that storage of digital information may be accomplished by the use of persistent supercurrents. Since the resistance of an element in the super state is identically zero, one may then store a circulating loop of current without any loss due to dissipation of energy by resistance. Another stated advantage of the cryotron element is its combined simplicity and versatility as a logical element, and the ease with which complicated logical functions can be synthesized with its use. The elementary cryotron functions as an element whose output is of the form "A and not B" where A represents the possibility of current flow through the gate element in the absence of control current, and B represents the presence of current in the control element [41].

Superconductive phenomena are essentially ideal for memory applications. Persistent supercurrents are a natural form of storage, and sharply defined thresholds between the superconductive and normal states permit switching. Moreover, thin superconductive film technology offers the possibility of simultaneous miniature batch fabrication of storage elements, addressing switches, and all connections. The superconductive memory can be used in a conventional semiconductor computer. The drivers for the cryotrons, the sense circuits, and the write and rewrite circuits are of the conventional transistor type. Here, however, in contrast to magnetic memories, the number of circuits increases only very moderately with capacity. For addressing drivers are necessary only for the binary bits of the address. The writing and sensing circuits need not be partitioned [94].

It is reasonable to expect that a large-scale digital computer would require less than one cubic foot of cryotrons. Because of the inexpensive raw materials and the simplicity of construction, the cost per bit is expected to be extremely low. Once a circuit is assembled, it will be exposed to almost ideal environment for the remainder of its life; an inert atmosphere at a temperature where all thermal activity has virtually ceased, electrically and thermally shielded from its surroundings [110].

Ittner [50] insists that it has not been possible to show that cryogenic circuits possess, on balance, any functional advantages over circuits realizable in competitive technologies. The principal costs in the cryogenic technology are found to lie largely in five areas,

namely: design, mask layout and checking; mask fabrication; circuit deposition; packaging; and refrigeration. The cryotronic technology, while possessing a number of special features, is functionally equivalent, on balance, to a number of existing technologies and must, therefore, be evaluated basically in terms of the function it can provide for a given cost.

B. Disadvantages

A rather remarkable revelation is that the literature, which is voluminous, deals very little with *disadvantages* of content-addressable and associative memory systems. One positive assertion by Fuller [30] is that floating point arithmetic is not efficient in content-addressable memories since it is necessary to sequentially normalize cell contents in the process of these operations. Considering the preponderance of applications concerned with high-level mathematical system solution, it would appear that this may be a rather awkward disadvantage to the mathematical scientist using a content-addressable hardware organization.

Cost of refrigeration for cryotron devices and problems existing in batch fabrication for both cryotronic and noncryotronic devices may be considered temporary disadvantages. As work accelerates in this field, cost factors will undoubtedly be drastically reduced, as they were with conventional memories.

It is difficult to say whether software needed for content-addressable organizations will be more or less complex. One can only say that it will be different from software generated for today's random-access computers. The removal of location addressing would inherently seem to simplify software housekeeping problems.

Recent experiments by Holt, et al. [45a] indicate that circuit switching times observed for crossed-film cryotrons are greater than those predicted from circuit time constant behavior of a simple step function cryotron switching model. Cryotron resistance does not appear in subnanosecond time as soon as the control current reaches the value required for switching the gate normal. Switching times are explained in terms of a model that accounts for observed cryotron switching delays. The model suggests that these delays (roughly 50 nanoseconds) can be largely overdriven by using as much as 50 per cent excess control current. Even then, noticeable switching delay is to be expected for circuit time constants much less than 100 nanoseconds, particularly for multistage circuits.

According to the report, cryotron circuit behavior is more complex than superficial considerations indicate, the circuit switching characteristics depend markedly on several strongly interrelated parameters, including switching current level, driving pulse shape, interaction between successive stages, geometry, and operating temperature.

IX. Summary

Content-addressable memories are those in which data may be located by content, rather than by specific address or location. The term "associative" in the sense of content-addressable systems refers to interrelationships between data, although this may imply a hardware organization in which neighboring cells are associated with each other.

Three concepts emerging from current research in the field are:

a) the content-addressable memory used as an auxiliary to a conventional memory;
b) the content-addressable memory used as a main memory for special purpose applications;
c) the "associative" processor, with content-addressable memory cells which have extended arithmetic and associative logic in addition to search and decision logic.

Although early work in content-addressable memories was accelerated by cryogenic or superconductive techniques, noncryogenic elements appear to offer comparable advantages without the need for costly refrigeration. Considerable investigation has been carried on with content-addressable techniques using tunnel diodes, ferrite ring cores, thin Permalloy films, crossed-film cryotrons, plated wire, Biax cores, BICORE thin films, and many other hardware elements.

Content-addressable memories are in general organized such that the "cell" is a collection of NDRO (nondestructive read-out) elements, word-organized, with some portion of the word reserved for data storage and the remainder reserved for "tagging" operations. Operations are generally those of searching for matches on equality, less than, greater than, and variations of between limits.

Memory cycle times have been reported as low as 50 nanoseconds, while command execution times for various memories range from 70 to over 700 nanoseconds for various operations. Current goals are indicated for operations speeds of 100–300 nanoseconds.

Memory costs have been estimated as low as $1.55 per cell for very large matrices and as high as $10 per bit. The outlook is for reduced hardware costs by the advent of new methods of fabrication. It is the consensus that costs will approach today's conventional memory costs in the near future.

Although the majority of research to date has been with small memories (up to 1000 cells), projections are indicated in the 10^7–10^8 bit range.

Novel software developments will be needed for use of content-addressable systems. It is indicated, however, that some of the complexity presently required for conventional location addressed memories will be minimized in content-addressable systems. Functions which can be performed with extended content-address-

able systems may be broadly classified into search, write, and read categories.

Applications suggested for content-addressable systems are numerous and include all aspects of file maintenance, pattern recognition, mathematical system solution, information storage and retrieval, translation, military operations, communication and transportation, and miscellaneous types.

Advantages of content-addressable memory organizations are increased data handling speeds, simplified software, and an organization which lends itself to batch fabrication techniques. Disadvantages are minimized in the literature.

Appendix

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