The Special Issue on High-Speed Memories

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Guest Editor

About this Issue

During the last few years, rapid advancement has occurred in the introduction and use of sophisticated digital computing systems. A key element of this progress has been the development of high performance internal memories. The demand for improved computing capability has increased in an exponential fashion as computer utilization spread into commercial, military, and industrial applications. As a result, a need has been created for memories with performance levels considered impossible a few years ago. Traditional approaches have been supplemented by new techniques made possible by advances in the materials sciences. The resulting new devices have been utilized by memory developers to mechanize and to organize memories which offer the systems engineer new levels of performance (increased speed, larger capacity, and lower cost).

For many years, the ferrite core has figured dominantly in the fabrication of internal memories. Only recently has this dominance been challenged. In fact, the majority of computers in operation today use ferrite core memories as the high-speed internal store. In the last year, however, we have seen delivery of thin-film memories in various forms, operating in systems that might otherwise have utilized core memories. Many of the promises long heralded for thin-film memories are on the threshold of being fulfilled in operating equipment in the field.

System-oriented approaches to computing applications have resulted in the emergence of a variety of special purpose memories: read-only, associative, very-high-speed control and scratchpad memories. Direct access mass memories show promise of being competitive, on a cost-performance basis, in those applications usually reserved for disk and drum. Based on a new organization, the $2\frac{1}{2}$D, these are in various stages of development or are in actual use in production equipment.

This period of time is an exciting one for those of us engaged in the memory field. It is a time when new techniques evolving from the laboratory promise improved performance, perhaps by an order of magnitude or more. We have been able to participate in and observe the evolution of these techniques from concept to working hardware. There is still much to be accomplished.

As the requirements for higher and higher volume of direct access storage increase, it appears that the production of memories from discrete storage elements will become economically infeasible. Consequently, new methods of mass and batch fabrication will be required to render these systems economically possible.

The selection of papers in this issue has been made with the intent to provide the reader with a sampling of developments in the areas memtioned. The papers

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deal with a variety of techniques, some presently practiced, some projected, and some on the horizon of memory technology. It is hoped that the following overview will indicate the variety and scope of the areas of current memory hardware development.

An Overview of the Issue

New Devices and Techniques

Integrated circuit memory arrays are an example of the application of new devices to the memory field. The ability to utilize monolithic silicon fabrication for large arrays of memory elements will permit logic at each cell location, a capability that was not practical with conventional devices. *Pleshko* and *Terman* of IBM describe the use of an MOS array used as a very-high-speed scratchpad memory. The paper is singular in that speeds quoted are significantly higher than those generally attributed to MOS arrays.

A paper by *Kriz* and *Ishii* of Marquette University discusses an experimental technique for nondestructive readout of ferrite cores. Using the bulk properties of ferrite, the authors propose a method for readout of information at very high speeds using an RF carrier technique. This approach is considered applicable to a mass memory configuration and may benefit from batch fabrication of the ferrite memory element.

Considerable work is presently underway in the device area of memory research utilizing multilayer films. Much of this effort is directed toward film pairs to enhance the nondestructive readout characteristics of storage elements. In this manner, composite properties are obtainable which are not characteristic of a single material or surface. *Matick* of IBM writes about a nondestructive readout memory device using thick magnetic films and discusses its use in a large high-speed memory array.

Film Memories

Maeda, *Matsushita*, and *Takashima* of Toko Coil of Japan present an engineering description of an NDRO memory system using rotationally switched permalloy plated wires with woven word lines. This technique is representative of a new class of film memories. The paper is further enhanced by a detailed description of the memory design considerations including noise problems, circuitry, and disturb and drive tolerance problems.

Pohm of Iowa State University discusses planar magnetic films and their application to reduced cost scratchpad memories. An interesting feature of this paper is an economic analysis of the cost breakpoints for various sizes and speeds. The discussion is particularly appropriate because film scratchpad memories, capable of very high speeds, are being challenged by integrated circuit memories for just this application.

The NCR 315 RMC is the first commercial computer to be delivered with a thin-film main memory. The thin-film "rod" is used as the memory element. *Higashi* of NCR describes this memory from an engineering point of view, and reviews the memory stack design, the circuitry, and the system organization. It is interesting to compare this memory to that of Toko Coil; both are in the same speed range, but they utilize basically different devices and stack construction.

Yao of GE presents a generalized analytic approach to the propagation of sense signals in large thin-film memory arrays. Equations are developed for attenuation, delay, and coupling in the array. As nearly everything in a high speed memory array is a transmission line, this type of analysis is a key to determining and to understanding its properties.

Ferrites

As proof that the ferrite memory field is very much alive, its proponents extremely active, and not the least bit inclined to give over its dominance to other techniques, *Gilligan* of Electronic Memories, Inc., reviews and extrapolates the characteristics of the $2\frac{1}{2}$D memory system. This major new approach to memory stack organization offers powerful advantages in cost-performance optimization of core memories. The $2\frac{1}{2}$D system makes possible mass core storage currently offered by several manufacturers and is clearly a technique which allows core memories to compete in the achievement of sub-microsecond speeds.

When faced with the actual task of selecting a core and an organizational mode for a memory design, the characteristics of the ferrite core, both primary and secondary, have much to do with the ultimate speed, size, and cost of the memory. The effect of these characteristics when used in 3D, $2\frac{1}{2}$D, or 2D organizations are reviewed and cataloged by *Brown* of Burroughs. Detailed discussion is offered regarding the relative importance and design impact of these factors in core selection.

Special Purpose Memories

A number of *application-oriented* memories are being developed which differ from the familiar conventionally organized random access systems (typified by core memories). Such memories are organized in a way uniquely suited to optimize the interface to the processor.

Aldrich and *Alonzo* of M.I.T. Instrumentation Laboratory describe a very large size read-only memory which is used as a control memory for a digital computer. While the memory uses ferrity elements for the actual storage, the mode of manufacture is unique. Their approach, weaving a complete memory array, is particularly attractive because the weaving may be easily altered to provide any possible combination of stored data by the use of a programmed loom.

Associative, or content-addressable memories are the subject of much current research, both theoretical and experimental. *Hanlon* of NCR presents a detailed and well-documented survey of this field, with some comments on both software and hardware considerations.

The theoretical description and analysis of an associative memory using cutpoint cells for storage locations is contained in a paper by *Yang* and *Yau* of Northwestern University. This type of memory is receiving increased attention from theoreticians and and hardware designers alike because mechanization using integrated circuit arrays is now within the realm of possibility.

A somewhat different approach to the associative memory is offered by *Sottile* and *Crofut* of Lockheed Electronics. A high-speed acoustic delay line is used in combination with ultra-high-speed logic for recirculation and access. The memory might best be described as word-serial and bit-parallel with circulating lines providing sequential storage.

As a finale, a review of the memory field as seen by a systems specialist, *Hobbs* of Hobbs Associates, considers the present state-of-the-art and makes some predictions and extrapolations as to techniques likely to become the future state-of-the-art within the next decade.

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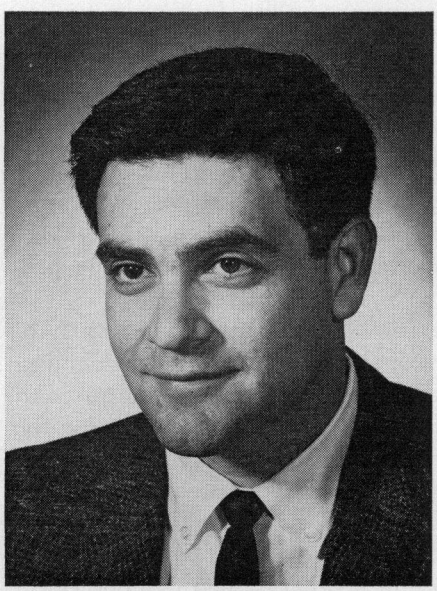

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In 1951 he joined The National Bureau of Standards as an Electronic Scientist, and subsequently has participated in such varied projects as electronic ordnance, air traffic control systems, digital and analog computing techniques, noise-correlation systems, and FM radar, in both government and industrial laboratories. His work at The National Cash Register Company has included contributions to the development of large high-speed thin-film memories, plated-wire memory devices, parametrons, nanosecond circuitry, and integrated circuit design and applications. One of the early workers in the thin-film memory field, he directed the team that guided the thin-film rod memory out of the laboratory and into the product stage. He is presently Head of the Computer Technology Section of the Research and Advanced Development Department at the Electronics Division of NCR, in Hawthorne, Calif., where he manages R & D activities in high speed memory systems and devices, ultra high speed computer techniques, thick-film circuitry, and integrated circuits.